基于 ARM Cortex-M3 处理器

与 FPGA 的实时人脸检测 SOC

软件配置手册

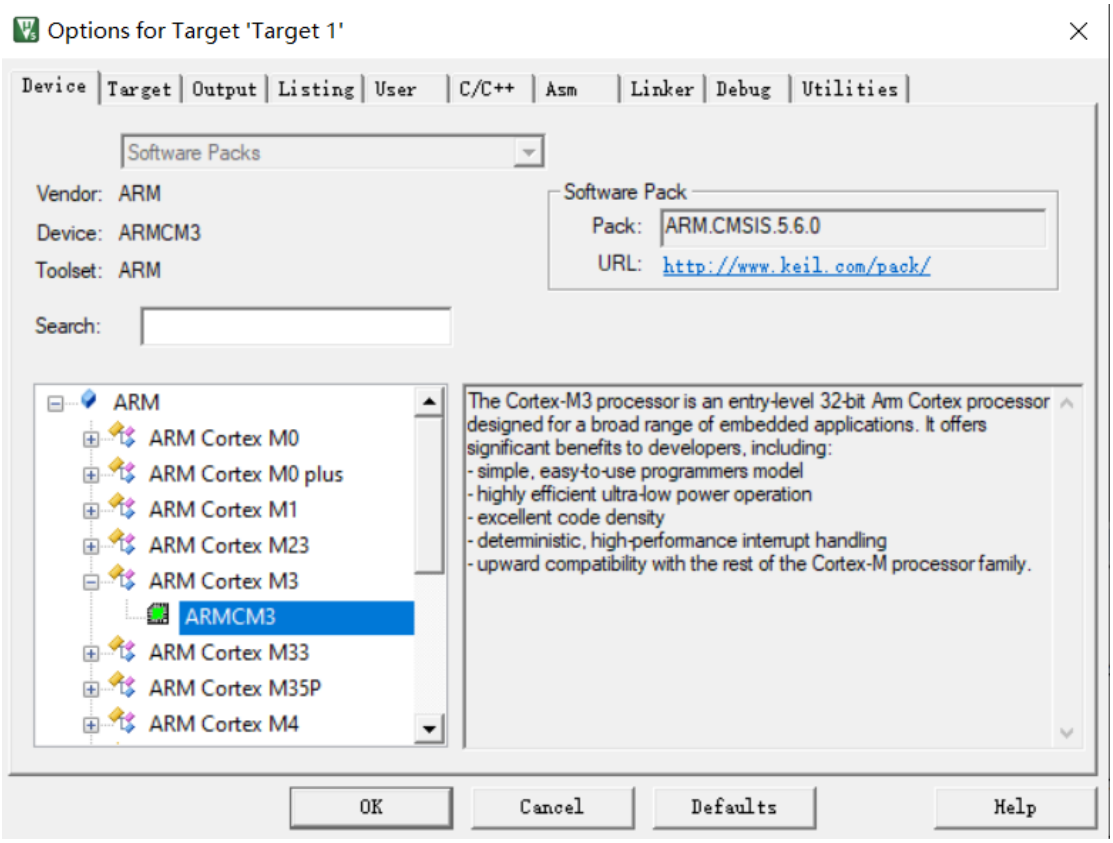
V1.0

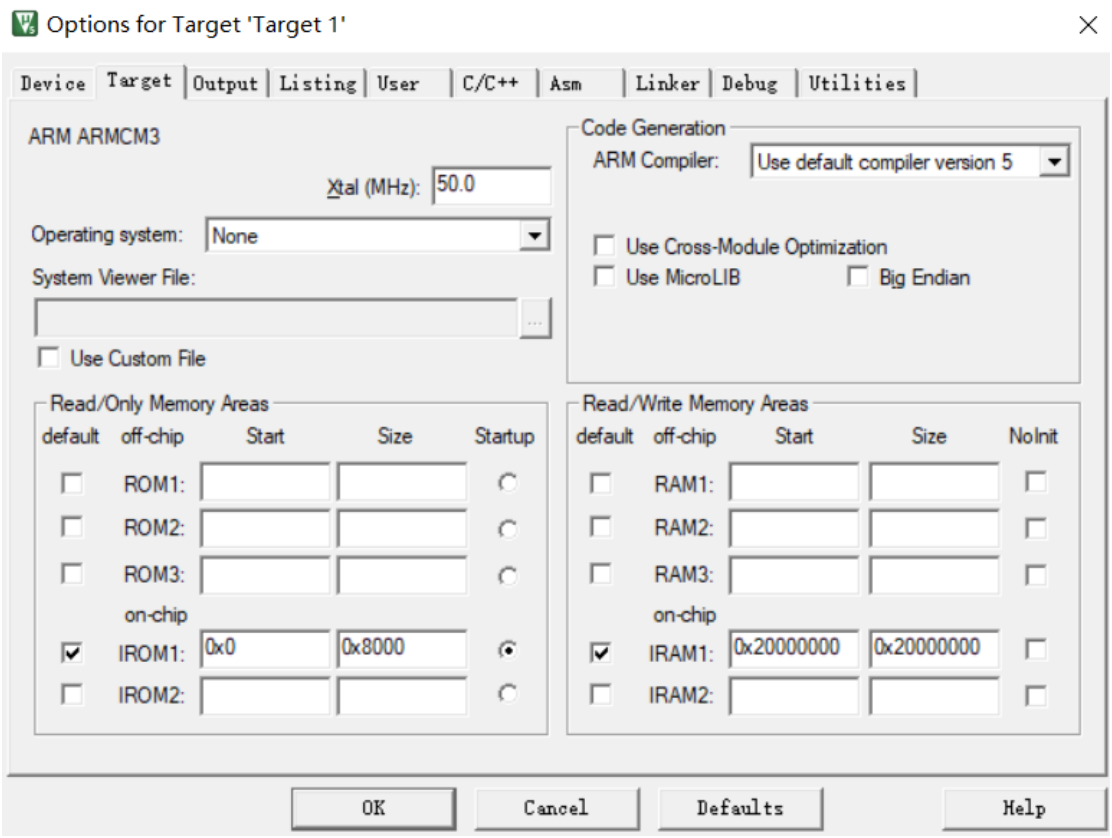
项目源代码访问：https://github.com/WalkerLau/DetectHumanFaces

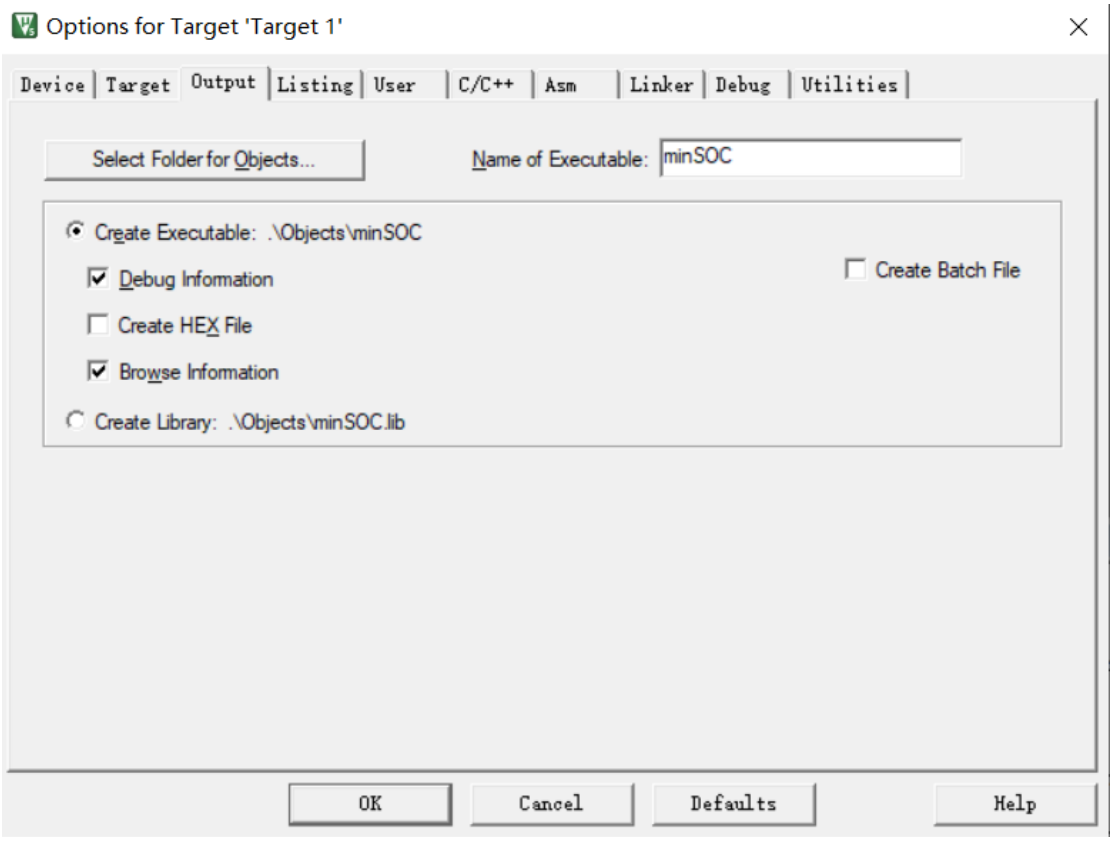
目录

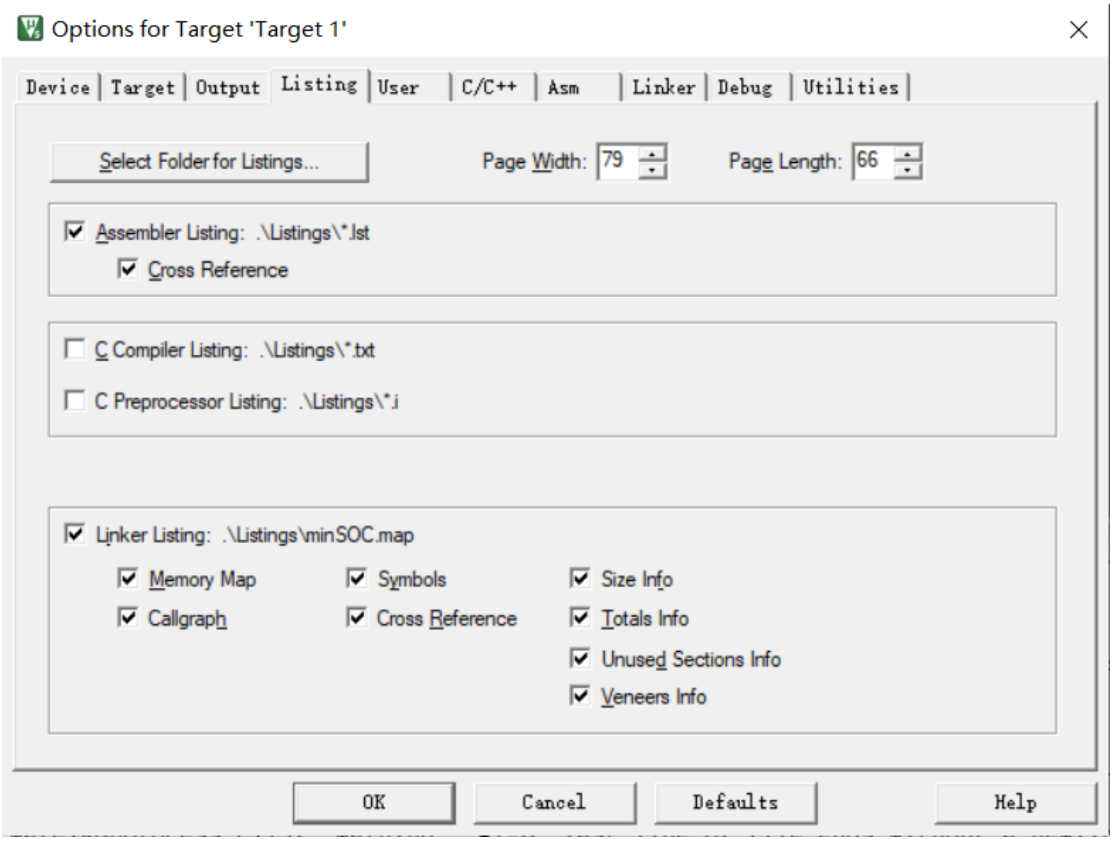
第一章　Keil 设置

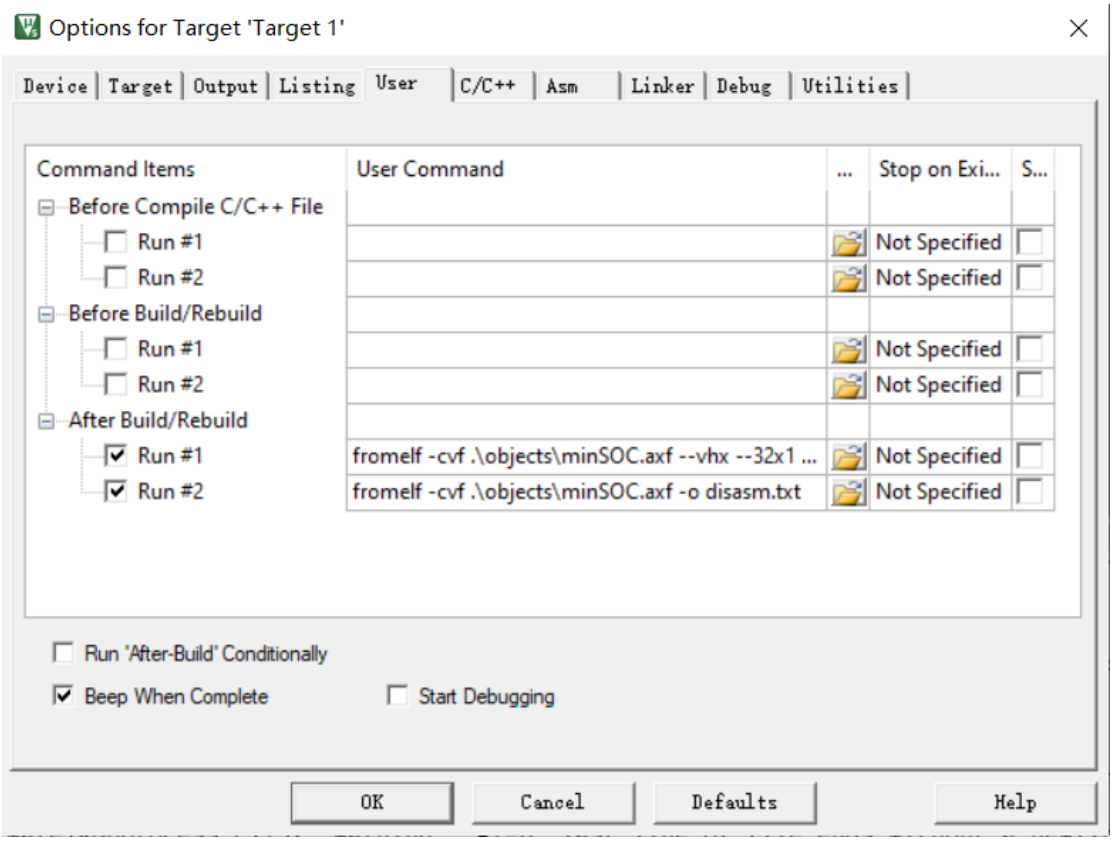
1.1 Options for target




Options for Target 'Target 1'
Device
Target
Output
Listing
User
C/C++
Asm
Linker
Debug
Utilities
ARM ARMCM3
Xtal (MHz): 50.0
Operating system: None
System Viewer File:
Use Custom File
Code Generation
ARM Compiler: Use default compiler version 5
Use Cross-Module Optimization
Use MicroLIB
Big Endian
Read/Only Memory Areas
default
off-chip
Start
Size
Startup
ROM1:
ROM2:
ROM3:
on-chip
IROM1: 0x0 0x8000
IROM2:
Read/Write Memory Areas
default
off-chip
Start
Size
NoInit
RAM1:
RAM2:
RAM3:
on-chip
IRAM1: 0x20000000 0x20000000
IRAM2:
OK
Cancel
Defaults
Help

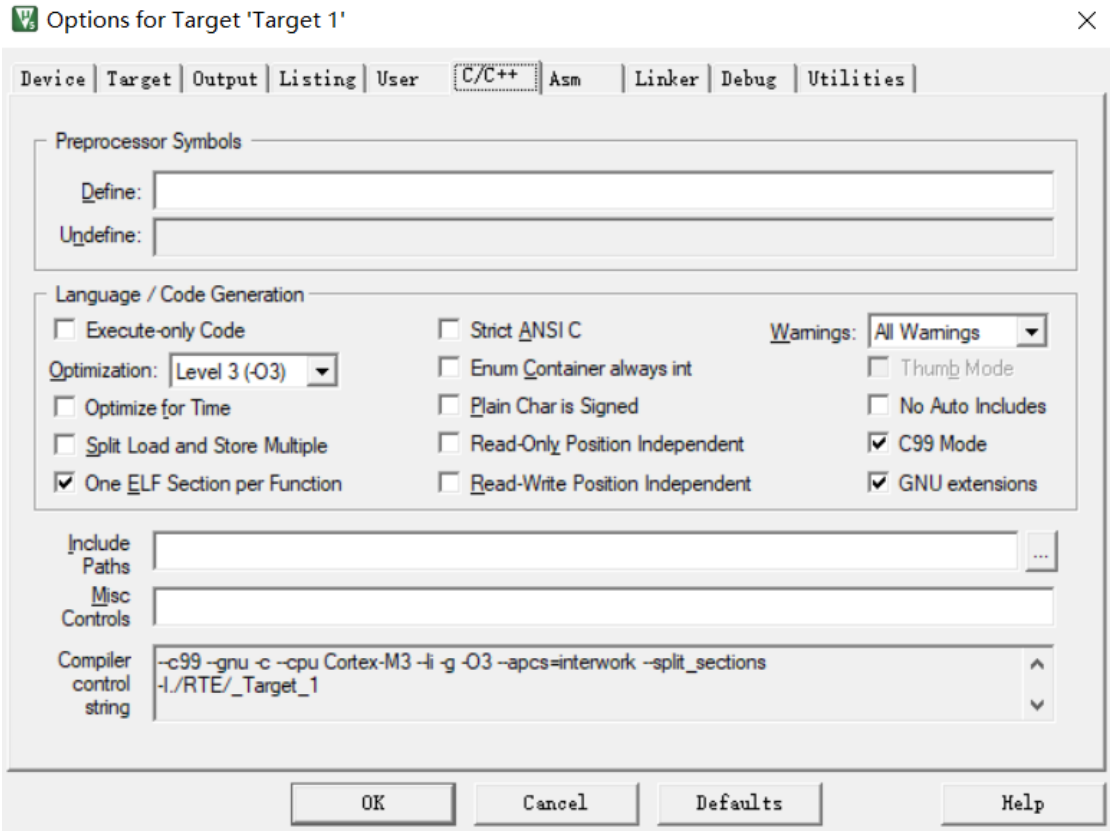

Options for Target 'Target 1'
Device
Target
Output
Listing
User
C/C++
Asm
Linker
Debug
Utilities
Select Folder for Objects...
Name of Executable: minSOC
Create Executable: .\Objects\minSOC
Debug Information
Create HEX File
Browse Information
Create Library: .\Objects\minSOC.lib
Create Batch File
OK
Cancel
Defaults
Help

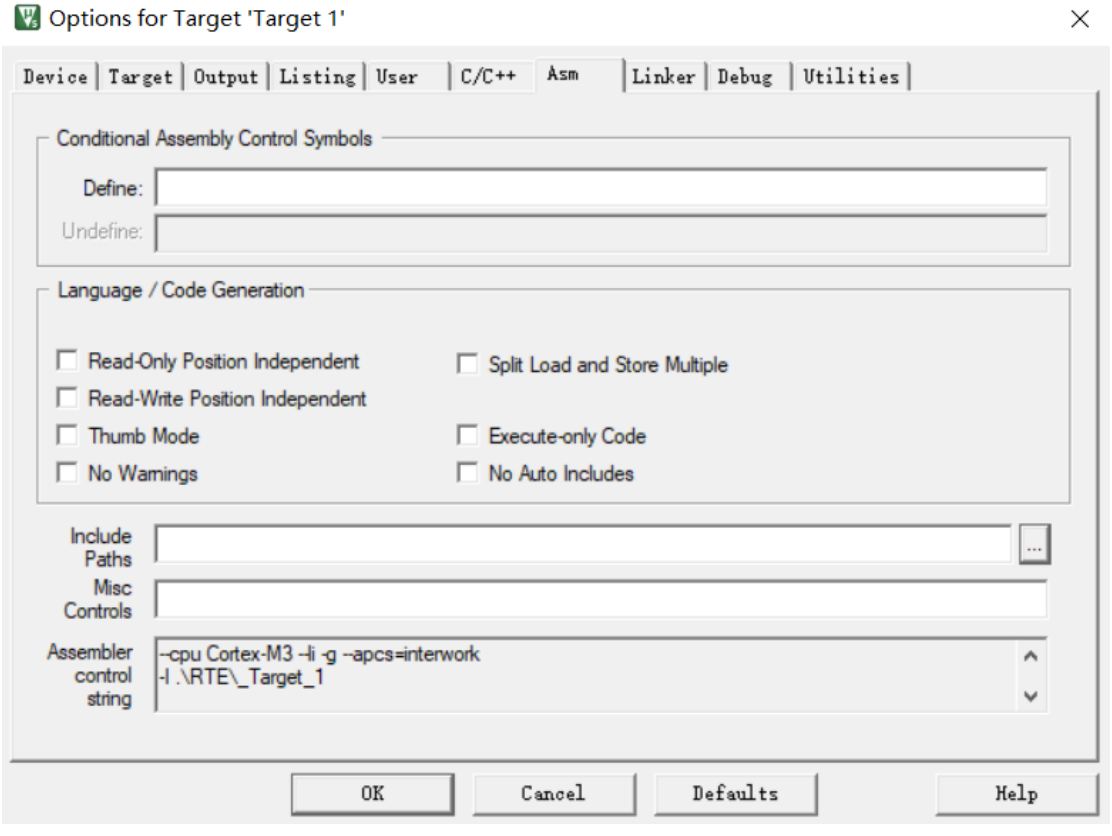


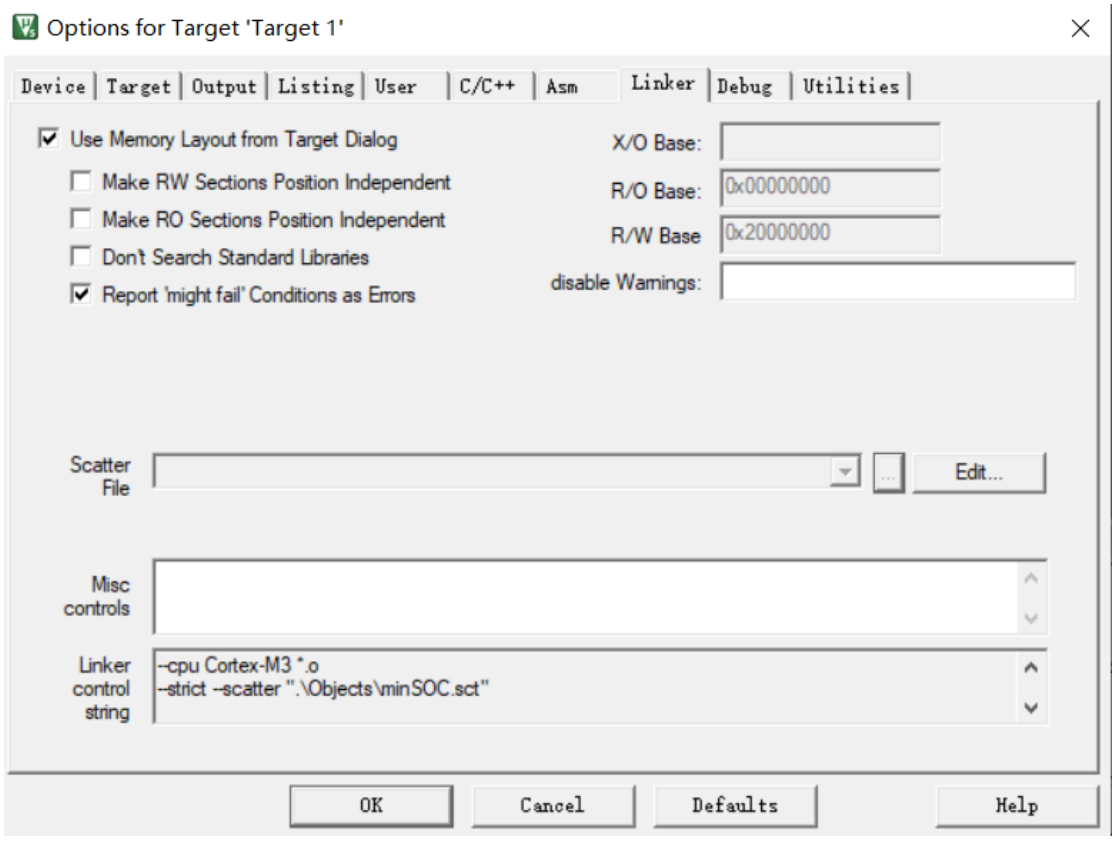


fromelf -cvf .\objects\minSOC.axf --vhx --32x1 -o minSOC.hex

fromelf -cvf .\objects\minSOC.axf -o disasm.txt

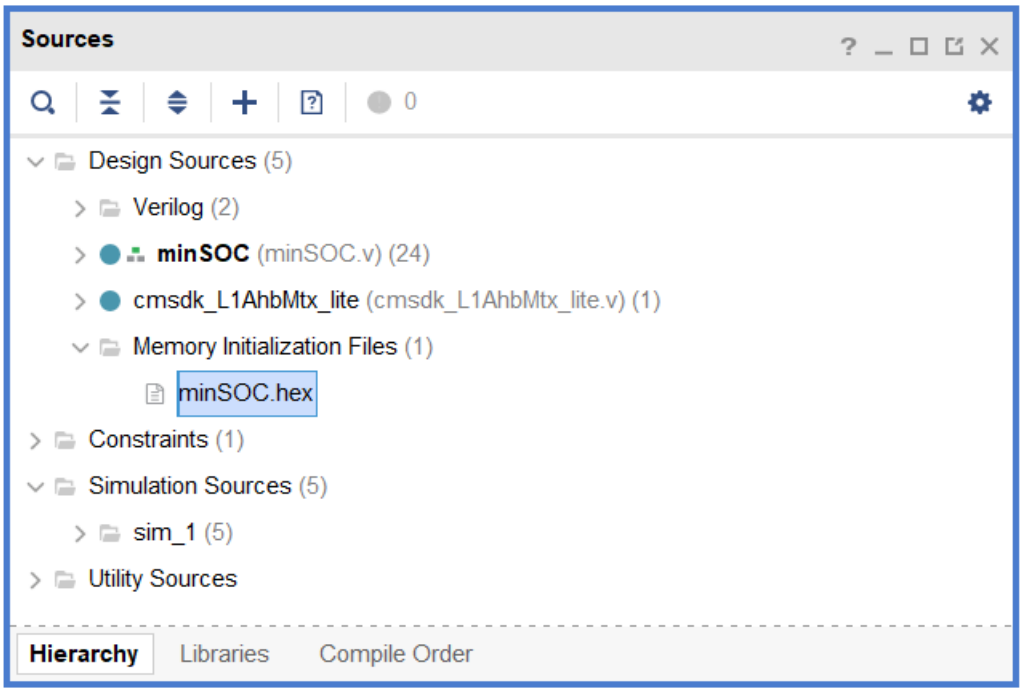

Options for Target 'Target 1'
Device
Target
Output
Listing
User
C/C++
Asm
Linker
Debug
Utilities
Preprocessor Symbols
Define:
Undefine:
Language / Code Generation
Execute-only Code
Strict ANSI C
Warnings:
All Warnings
Optimization:
Level 3 (-O3)
Enum Container always int
Thumb Mode
Optimize for Time
Plain Char is Signed
No Auto Includes
Split Load and Store Multiple
Read-Only Position Independent
C99 Mode
One ELF Section per Function
Read-Write Position Independent
GNU extensions
Include Paths
Misc Controls
Compiler control string
--c99 --gnu -c --cpu Cortex-M3 -li -g -O3 --apcs=interwork --split_sections
-I./RTE/_Target_1
OK
Cancel
Defaults
Help

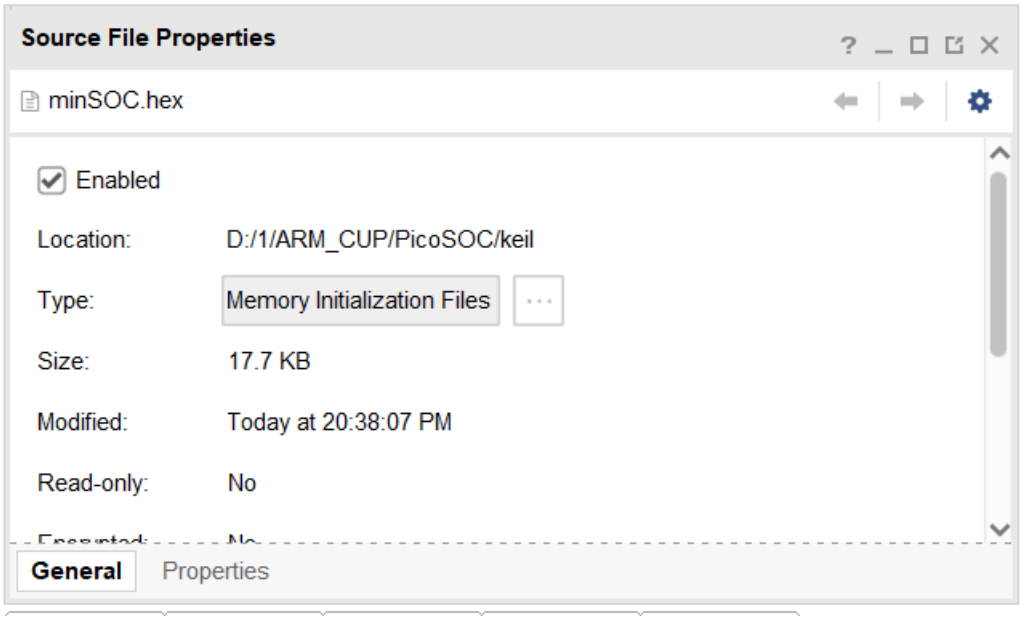

Options for Target 'Target 1'
Device
Target
Output
Listing
User
C/C++
Asm
Linker
Debug
Utilities
Conditional Assembly Control Symbols
Define:
Undefine:
Language / Code Generation
Read-Only Position Independent
Split Load and Store Multiple
Read-Write Position Independent
Thumb Mode
Execute-only Code
No Warnings
No Auto Includes
Include Paths
Misc Controls
Assembler control string
--cpu Cortex-M3 -li -g --apcs=interwork
-I .\RTE_Target_1
OK
Cancel
Defaults
Help


Options for Target 'Target 1'
Device
Target
Output
Listing
User
C/C++
Asm
Linker
Debug
Utilities
Use Memory Layout from Target Dialog
Make RW Sections Position Independent
Make RO Sections Position Independent
Don't Search Standard Libraries
Report 'might fail' Conditions as Errors
X/O Base:
R/O Base:
0x00000000
R/W Base
0x20000000
disable Warnings:
Scatter File
Edit...
Misc controls
Linker control string
--cpu Cortex-M3 *.o
--strict --scatter ".\Objects\minSOC.sct"
OK
Cancel
Defaults
Help

第二章　Vivado ip 设置

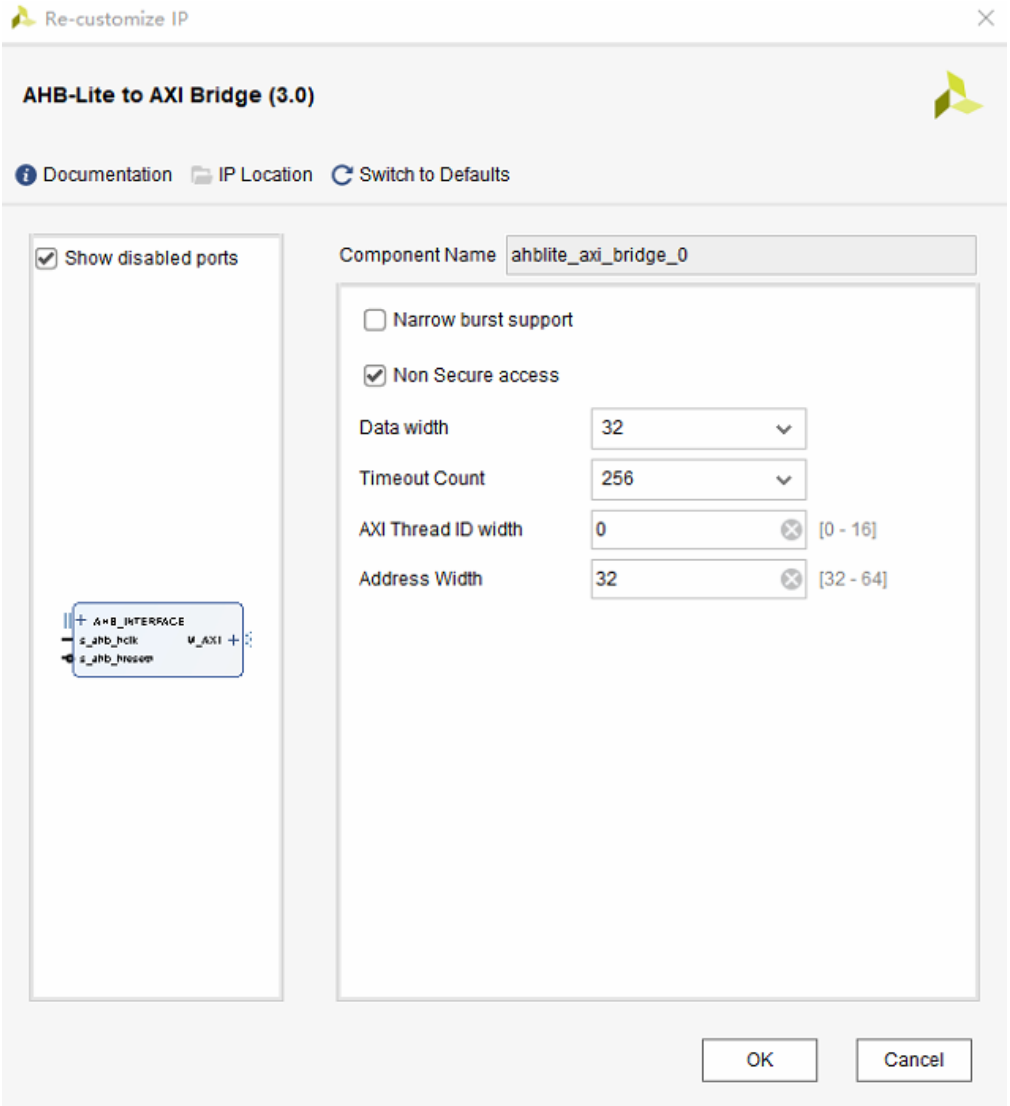
2.1 添加文件



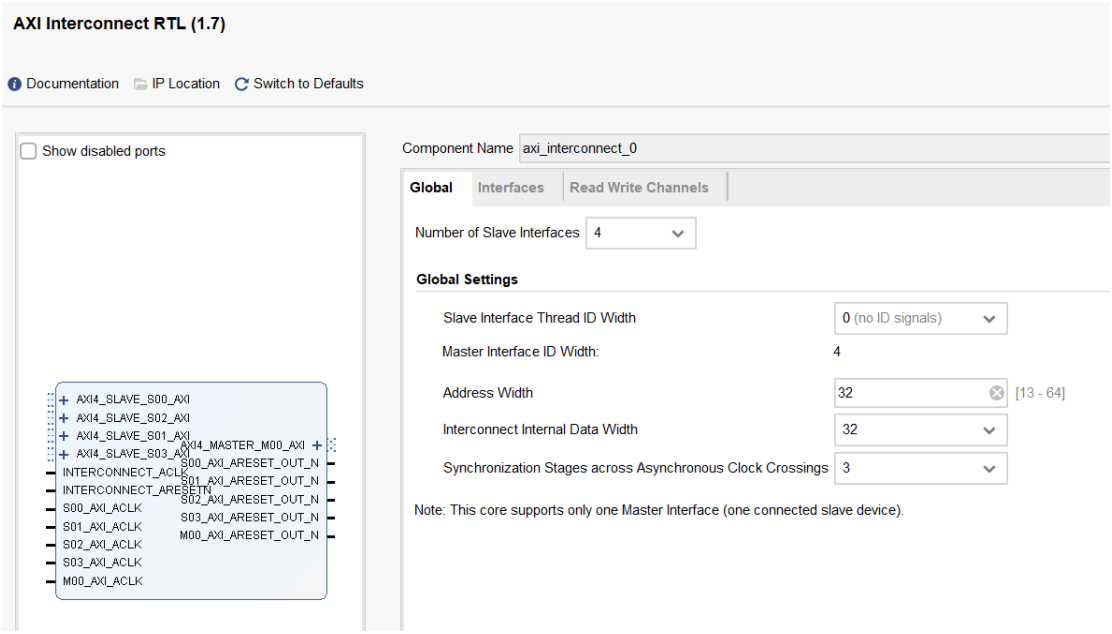


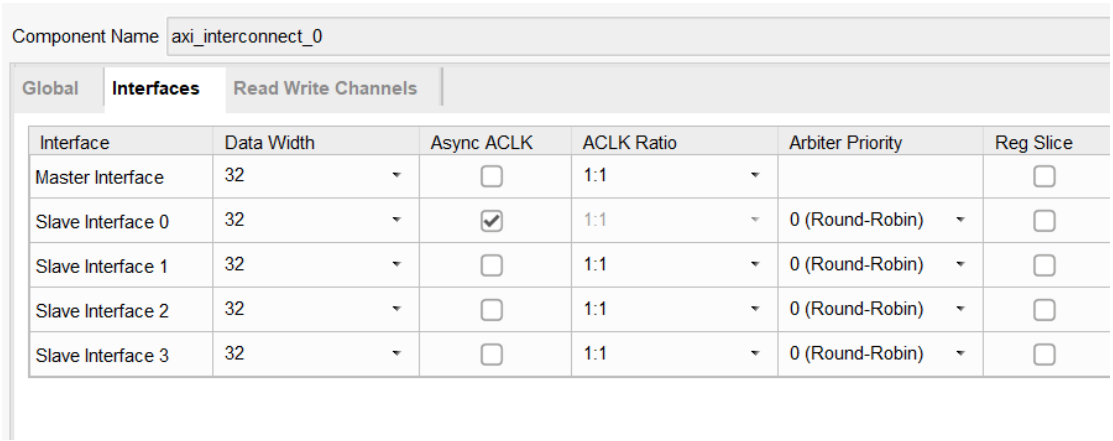
主要是添加由 keil 编译得到的 hex 可执行文件（minSOC.hex），并设置为 memory initialization files。

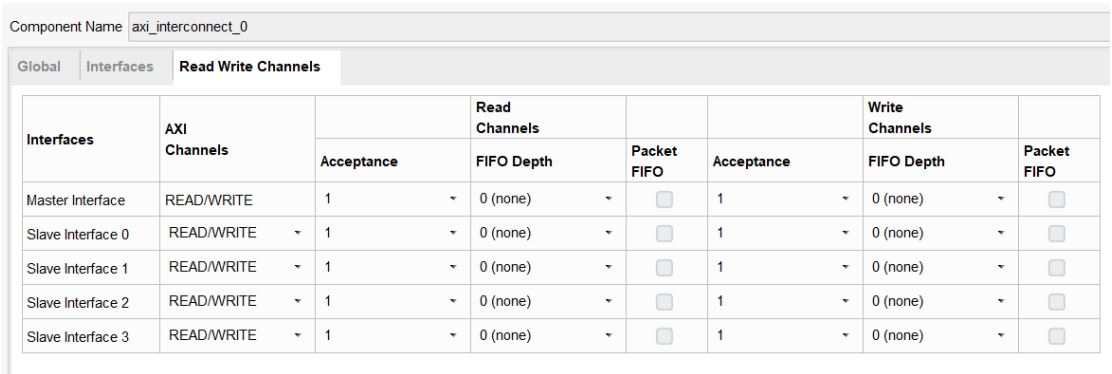
2.2 AHB-Lite to AXI Bridge



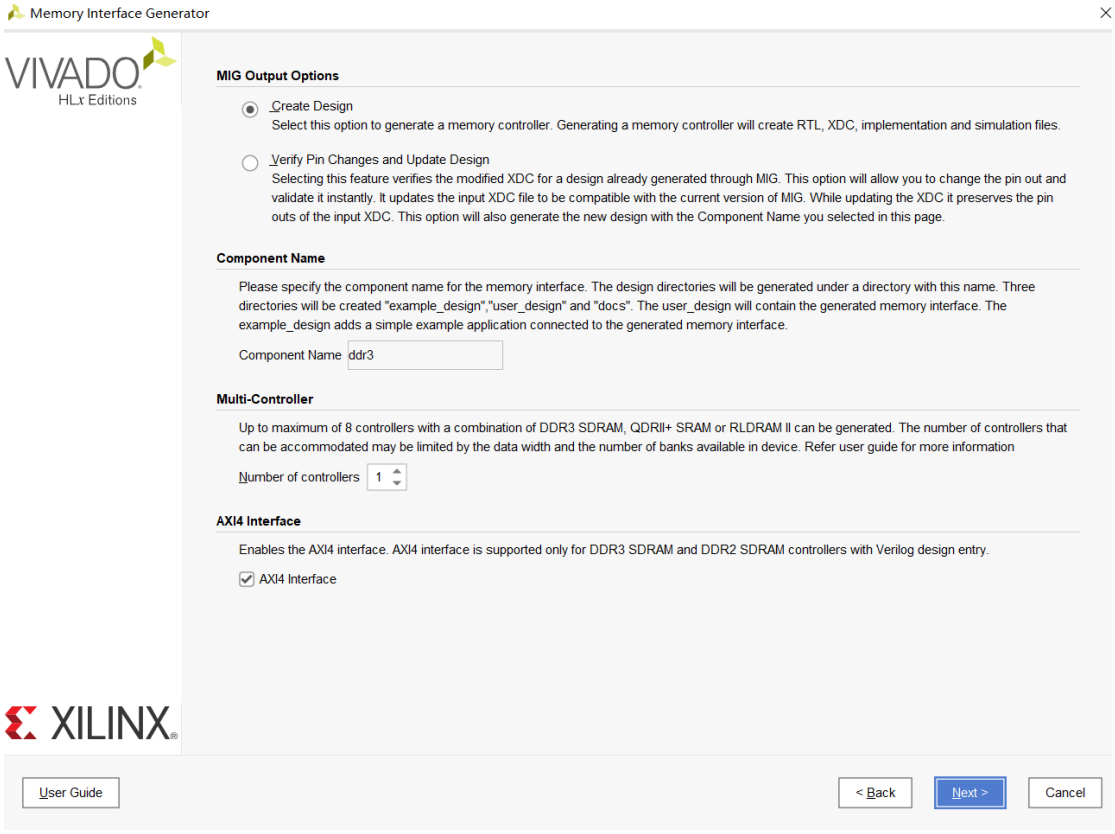
2.3 AXI Interconnect RTL

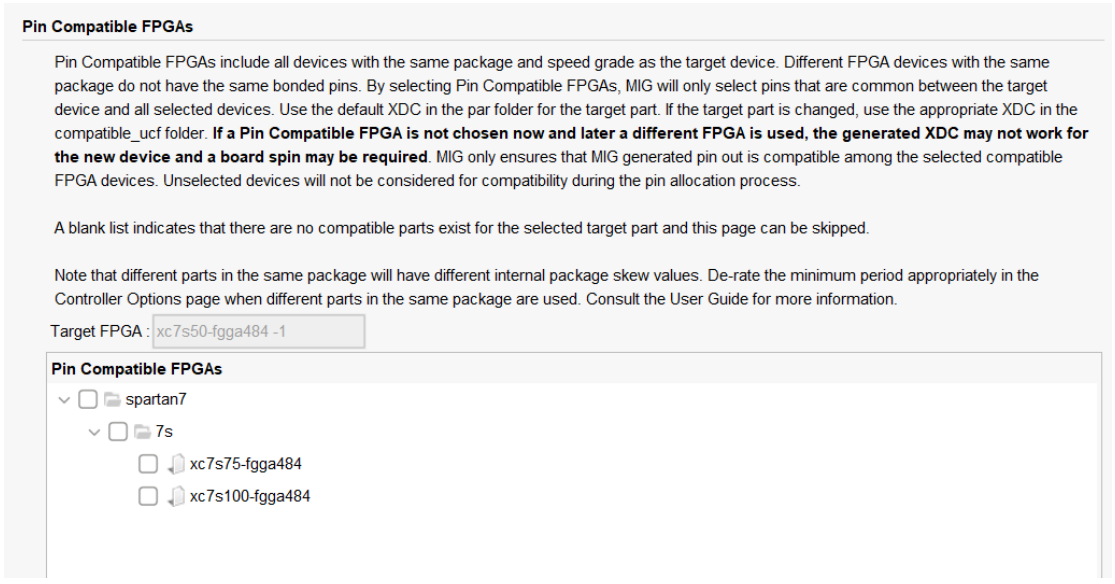






2.4 MIG


Memory Interface Generator
VIVADO
HLx Editions
MIG Output Options
Create Design
Select this option to generate a memory controller. Generating a memory controller will create RTL, XDC, implementation and simulation files.
Verify Pin Changes and Update Design
Selecting this feature verifies the modified XDC for a design already generated through MIG. This option will allow you to change the pin out and validate it instantly. It updates the input XDC file to be compatible with the current version of MIG. While updating the XDC it preserves the pin outs of the input XDC. This option will also generate the new design with the Component Name you selected in this page.
Component Name
Please specify the component name for the memory interface. The design directories will be generated under a directory with this name. Three directories will be created "example_design","user_design" and "docs". The user_design will contain the generated memory interface. The example_design adds a simple example application connected to the generated memory interface.
Component Name ddr3
Multi-Controller
Up to maximum of 8 controllers with a combination of DDR3 SDRAM, QDRII+ SRAM or RLDRAM II can be generated. The number of controllers that can be accommodated may be limited by the data width and the number of banks available in device. Refer user guide for more information
Number of controllers 1
AXI4 Interface
Enables the AXI4 interface. AXI4 interface is supported only for DDR3 SDRAM and DDR2 SDRAM controllers with Verilog design entry.
AXI4 Interface
XILINX
User Guide
< Back
Next >
Cancel


Pin Compatible FPGAs
Pin Compatible FPGAs include all devices with the same package and speed grade as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. Use the default XDC in the par folder for the target part. If the target part is changed, use the appropriate XDC in the compatible_ucf folder. If a Pin Compatible FPGA is not chosen now and later a different FPGA is used, the generated XDC may not work for the new device and a board spin may be required. MIG only ensures that MIG generated pin out is compatible among the selected compatible FPGA devices. Unselected devices will not be considered for compatibility during the pin allocation process.
A blank list indicates that there are no compatible parts exist for the selected target part and this page can be skipped.
Note that different parts in the same package will have different internal package skew values. De-rate the minimum period appropriately in the Controller Options page when different parts in the same package are used. Consult the User Guide for more information.
Target FPGA : xc7s50-fgga484 -1
Pin Compatible FPGAs
spartan7
7s
xc7s75-fgga484
xc7s100-fgga484

Memory Selection

Select the type of memory interface. Please refer to the User Guide for a detailed list of supported controllers for each FPGA family. The list below shows currently available interface(s) for the specific FPGA, speed grade and design entry chosen.

Select the controller type:

- (●) **DDR3 SDRAM**
- ( ) **DDR2 SDRAM**

Options for Controller 0 - DDR3 SDRAM

Clock Period: Choose the clock period for the desired frequency. The allowed period range(**3000 - 3300**) is a function of the selected FPGA part and FPGA speed grade. Refer to the User Guide for more information.

3,077 ps 324.99 MHz

PHY to Controller Clock Ratio: Select the PHY to Memory Controller clock ratio. The PHY operates at the Memory Clock Period chosen above. The controller operates at either 1/4 or 1/2 of the PHY rate. The selected Memory Clock Period will limit the choices.

4:1

Vccaux_io: Vccaux_io must be set to 2.0V in the High Performance banks for the highest data rates. Vccaux_io is not available in the High Range banks. Note that Vccaux_io is common to groups of banks. Consult the 7 Series Datasheets and FPGA SelectIO Resources User Guide for more information.

1.8V

Memory Type: Select the memory type. Type(s) marked with a warning symbol are not compatible with the frequency selection above.

Components

Memory Part: Select the memory part. Part(s) marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part needed is not listed here. The "Create Custom Part" feature is not supported for RLDRAM II.

MT41J256m16XX-125

Create Custom Part

Memory Voltage: Select the Voltage of the Memory part selected.

1.5V

Data Width: Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above.

32

ECC: MIG supports ECC for 72 bit data width configuration. To be able to select ECC, select a data width that has ECC supported.

Disabled

Data Mask: Enable or disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part selected has DM pins. Uncheck this box to not use data masks and save FPGA I/Os

ECC: MIG supports ECC for 72 bit data width configuration. To be able to select ECC, select a data width that has ECC supported.

Disabled

Data Mask: Enable or disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part selected has DM pins. Uncheck this box to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs (DDR3 SDRAM, DDR2 SDRAM) will not use Data Mask.

Number of Bank Machines: This parameter defines the number of bank machines. A given bank machine manages a single DRAM bank at any given time.
Note:Setting a lower value will result in lower resource utilization, but may effect controller efficiency for certain traffic patterns.

8

ORDERING: Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received.

Normal

Memory Details: 4Gb, x16, row:15, col:10, bank:3, data bits per strobe:8, with data mask, single rank, 1.5V

Axi Parameter Options C0 - DDR3 SDRAM

Data Width

AXI DATA WIDTH: Data width of AXI read & write channels. The data width is less than or equal to user interface data width with the possible values 32, 64, 128, 256 & 512.

32

Arbitration Scheme

Select the arbitration scheme between the read and write address channels

RD_PRI_REG_STARVE_LIMIT

Narrow Burst Support

Enables logic to support narrow bursts on the AXI4 slave interface. Can be set to zero if no masters in the system issue narrow bursts and all the data widths are equal. (1-Enable, 0-Disable)

0

Address Width

AXI4 address width of read and write address channels.

30

ID Width

AXI4 ID width for read and write channels. AXI4 ID is used as the identification tag for write or read address group of signals

4

Memory Options C0 - DDR3 SDRAM

Input Clock Period: Select the period for the PLL input clock (CLKIN). MIG determines the allowable input clock periods based on the Memory Clock Period entered above and the clocking guidelines listed in the User Guide. The generated design will use the selected Input Clock and Memory Clock Periods to generate the required PLL parameters. If the required input clock period is not available, the Memory Clock Period must be modified.

5000 ps (200 MHz)

Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.

Read Burst Type and Length

The burst type determines the data ordering within a burst. Consult the memory datasheet for more information. Burst length 8 is the only supported value.

Sequential

Output Driver Impedance Control

Programmable impedance for the output buffer.

RZQ/7

RTT (nominal) - On Die Termination (ODT)

Select the nominal value of ODT for the DQ, DQS/DQS# and DM signals on the component or DIMM interface. This must be set to RZQ/6 i(40 ohms) for data rates at 1333 Mbps and above. In 2 slot DIMM configuations this value will be used for the unwritten slot during a write and will also be used for the unselected slot during a read. Use board level simulation to choose the optimum value.

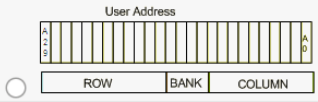
RZQ/4

Controller Chip Select Pin

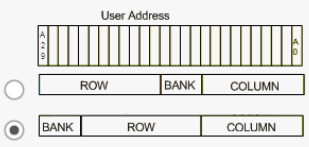
The Chip Select (CS#) pin can be tied low externally to save one pin in the address/command group when this selection is set to 'Disable'. Disable is only valid for single rank configurations.

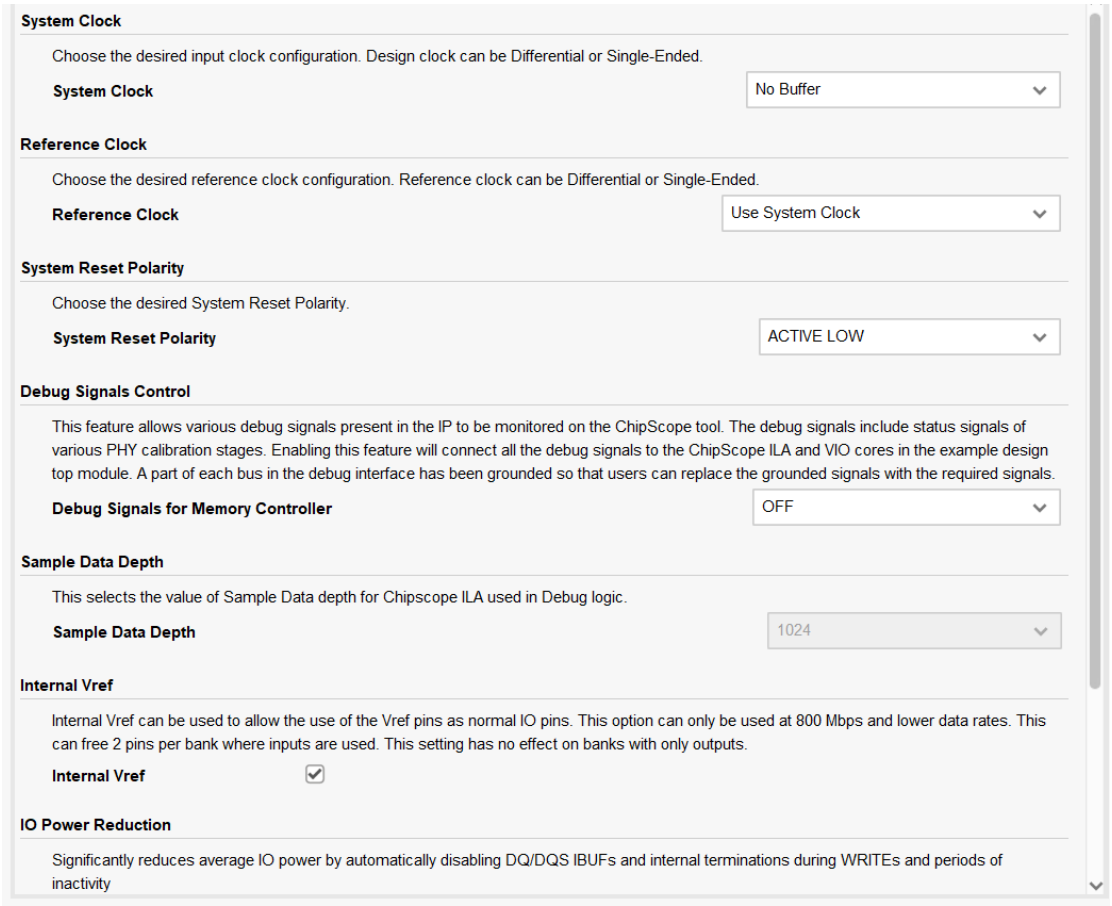
Enable

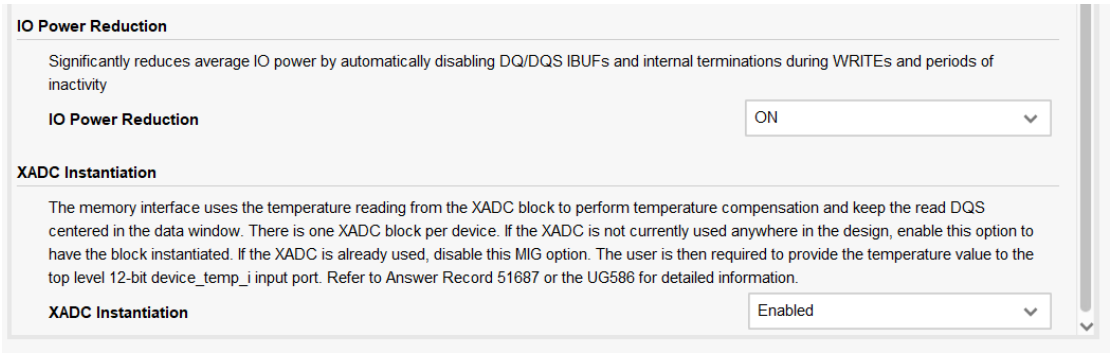
Memory Address Mapping Selection

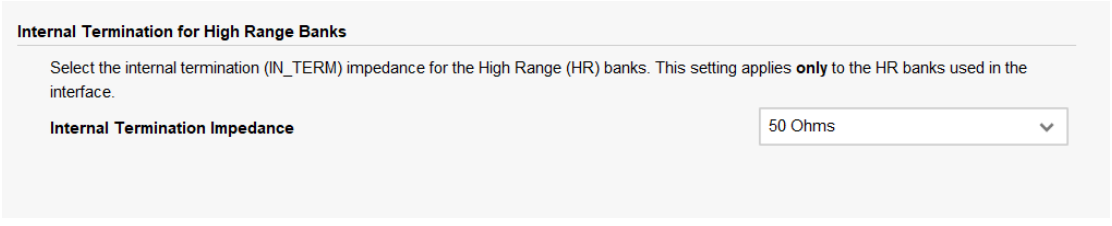


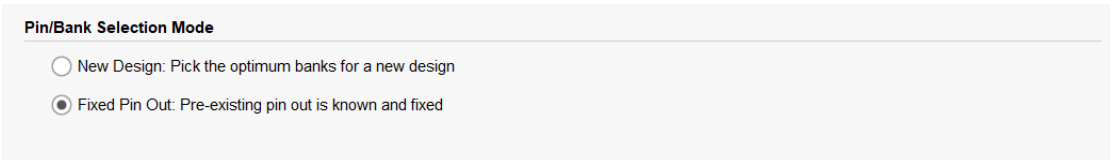
Memory Address Mapping Selection



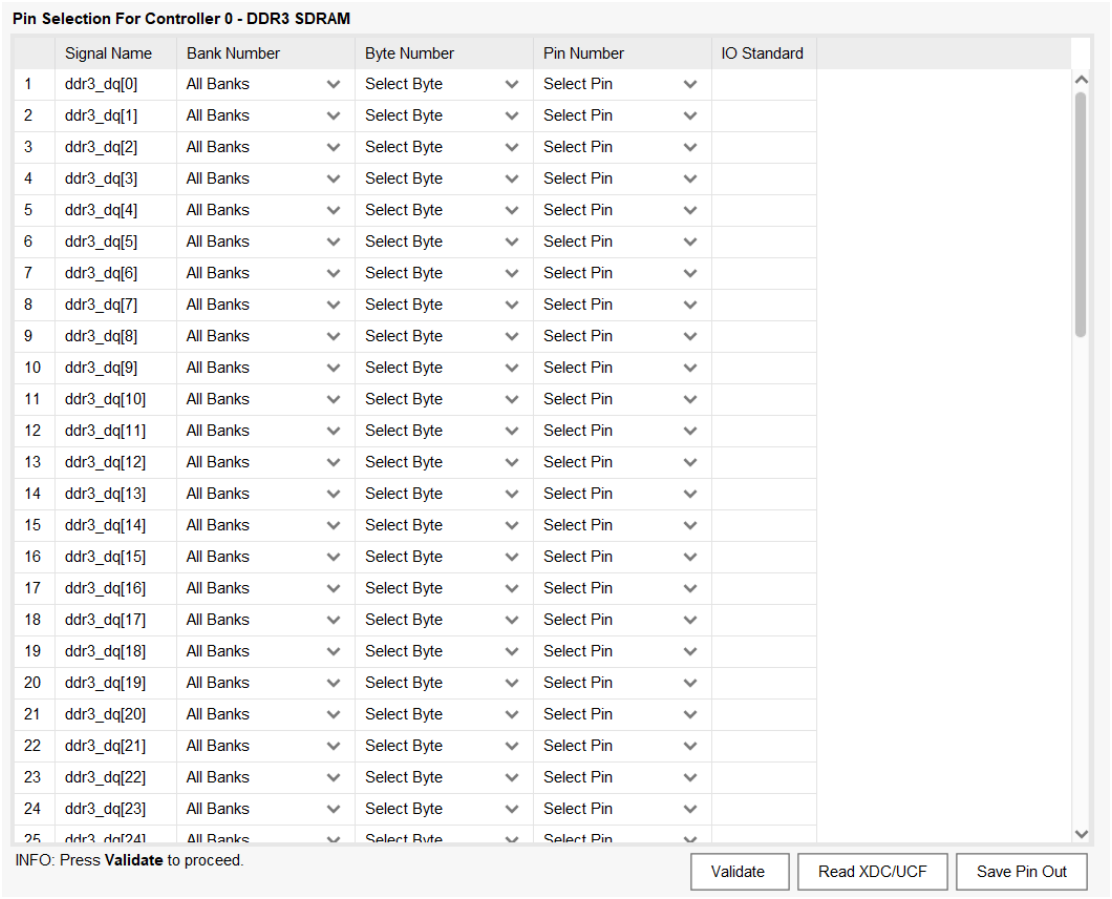

System Clock
Choose the desired input clock configuration. Design clock can be Differential or Single-Ended.
System Clock
No Buffer
Reference Clock
Choose the desired reference clock configuration. Reference clock can be Differential or Single-Ended.
Reference Clock
Use System Clock
System Reset Polarity
Choose the desired System Reset Polarity.
System Reset Polarity
ACTIVE LOW
Debug Signals Control
This feature allows various debug signals present in the IP to be monitored on the ChipScope tool. The debug signals include status signals of various PHY calibration stages. Enabling this feature will connect all the debug signals to the ChipScope ILA and VIO cores in the example design top module. A part of each bus in the debug interface has been grounded so that users can replace the grounded signals with the required signals.
Debug Signals for Memory Controller
OFF
Sample Data Depth
This selects the value of Sample Data depth for Chipscope ILA used in Debug logic.
Sample Data Depth
1024
Internal Vref
Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This option can only be used at 800 Mbps and lower data rates. This can free 2 pins per bank where inputs are used. This setting has no effect on banks with only outputs.
Internal Vref
IO Power Reduction
Significantly reduces average IO power by automatically disabling DQ/DQS IBUFs and internal terminations during WRITEs and periods of inactivity


IO Power Reduction
Significantly reduces average IO power by automatically disabling DQ/DQS IBUFs and internal terminations during WRITEs and periods of inactivity
IO Power Reduction
ON
XADC Instantiation
The memory interface uses the temperature reading from the XADC block to perform temperature compensation and keep the read DQS centered in the data window. There is one XADC block per device. If the XADC is not currently used anywhere in the design, enable this option to have the block instantiated. If the XADC is already used, disable this MIG option. The user is then required to provide the temperature value to the top level 12-bit device_temp_i input port. Refer to Answer Record 51687 or the UG586 for detailed information.
XADC Instantiation
Enabled


Internal Termination for High Range Banks
Select the internal termination (IN_TERM) impedance for the High Range (HR) banks. This setting applies only to the HR banks used in the interface.
Internal Termination Impedance
50 Ohms


Pin/Bank Selection Mode
New Design: Pick the optimum banks for a new design
Fixed Pin Out: Pre-existing pin out is known and fixed

选择 Read XDC/UCF，读取 DDR 约束文件（ddr3.ucf），然后按 validate，然后下一步：



Pin Selection For Controller 0 - DDR3 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	35	T0	H2	SSTL15
2	ddr3_dq[1]	35	T0	K2	SSTL15
3	ddr3_dq[2]	35	T0	H3	SSTL15
4	ddr3_dq[3]	35	T0	H6	SSTL15
5	ddr3_dq[4]	35	T0	H5	SSTL15
6	ddr3_dq[5]	35	T0	K6	SSTL15
7	ddr3_dq[6]	35	T0	H4	SSTL15
8	ddr3_dq[7]	35	T0	J3	SSTL15
9	ddr3_dq[8]	35	T1	M8	SSTL15
10	ddr3_dq[9]	35			
11	ddr3_dq[10]	35			
12	ddr3_dq[11]	35			
13	ddr3_dq[12]	35			
14	ddr3_dq[13]	35			
15	ddr3_dq[14]	35			
16	ddr3_dq[15]	35	T1	J7	SSTL15
17	ddr3_dq[16]	35	T2	L1	SSTL15
18	ddr3_dq[17]	35	T2	P3	SSTL15
19	ddr3_dq[18]	35	T2	K1	SSTL15
20	ddr3_dq[19]	35	T2	N4	SSTL15
21	ddr3_dq[20]	35	T2	N1	SSTL15
22	ddr3_dq[21]	35	T2	P1	SSTL15
23	ddr3_dq[22]	35	T2	M3	SSTL15
24	ddr3_dq[23]	35	T2	N3	SSTL15
25	ddr3_dq[24]	35	T3	R4	SSTL15

DRC Validation

Current Pinout is valid.

Save Log Message... OK

INFO: Press **Validate** to proceed.

Validate Read XDC/UCF Save Pin Out

默认，下一步：

System Signals Selection

Select the system pins below appropriately for the interface. Customization of these pins can also be made in the XDC after the design is generated. For more information see UG586 Bank and Pin rules.

System Clock and Reference Clock pin selections will not be visible if the 'No Buffer' option was selected in the FPGA Options page.

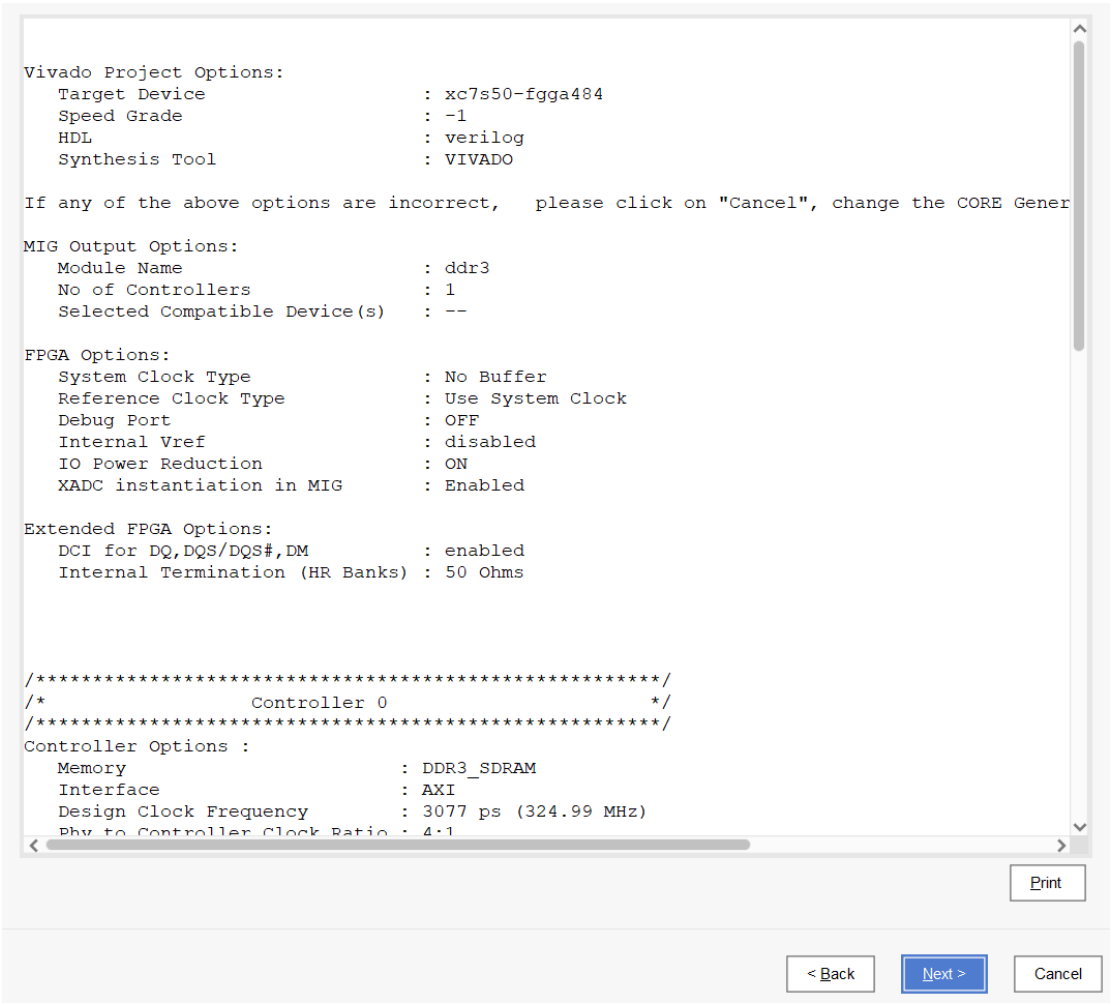
System Signals

These signals may be connected internally to other logic or brought out to a pin.

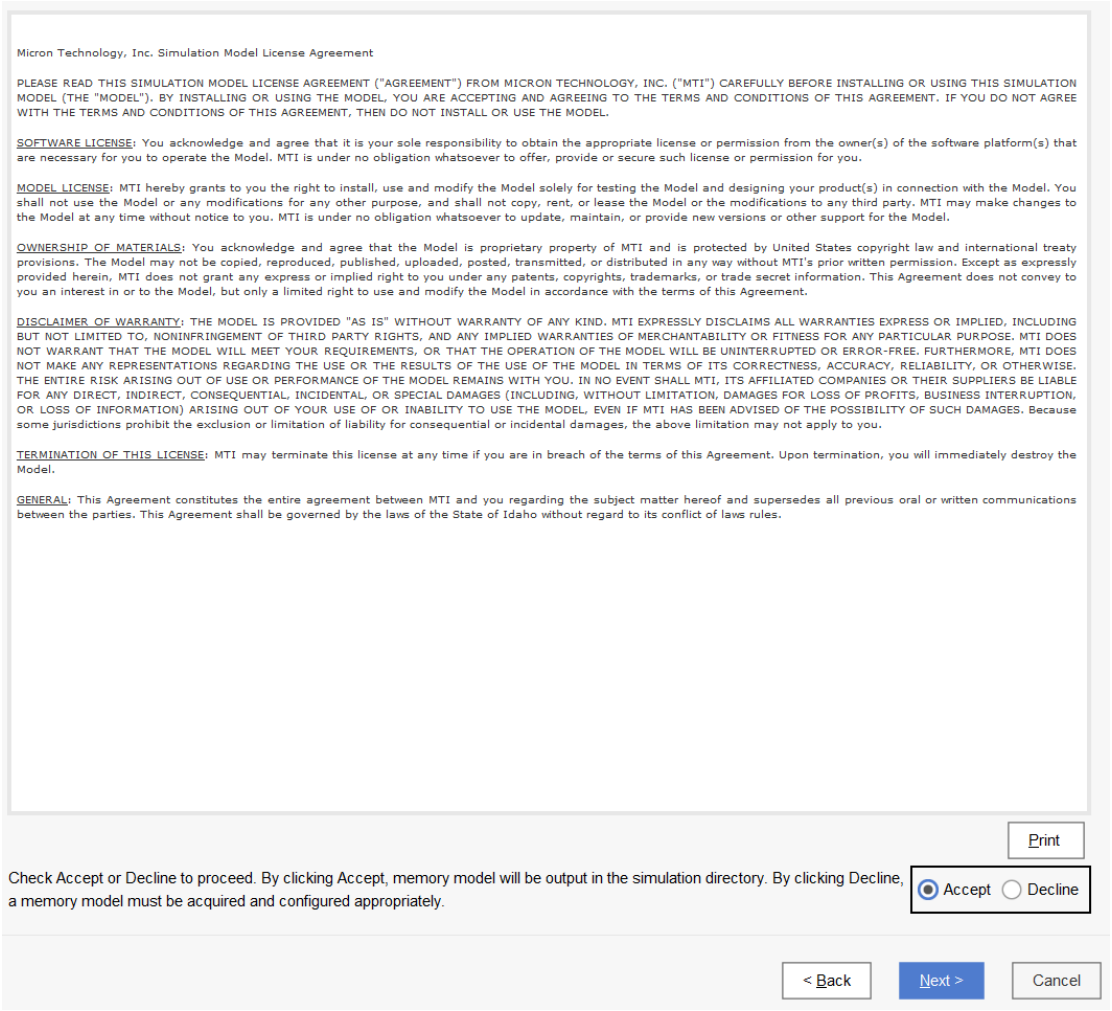
- **sys_rst**: This input signal is used to reset the interface.
- **init_calib_complete**: This signal indicates that the interface has completed calibration and memory initialization and is ready for commands. LOC constraint will be generated in XDC for Example design only based on "Pin Number" selection below.
- **error**: This output signal indicates that the traffic generator in the Example Design has detected a data mismatch. This signal does not exist in the User Design.

Signal Name	Bank Number	Pin Number
sys_rst	Select Bank	No connect
init_calib_complete	Select Bank	No connect
tg_compare_error	Select Bank	No connect

总结，下一步：

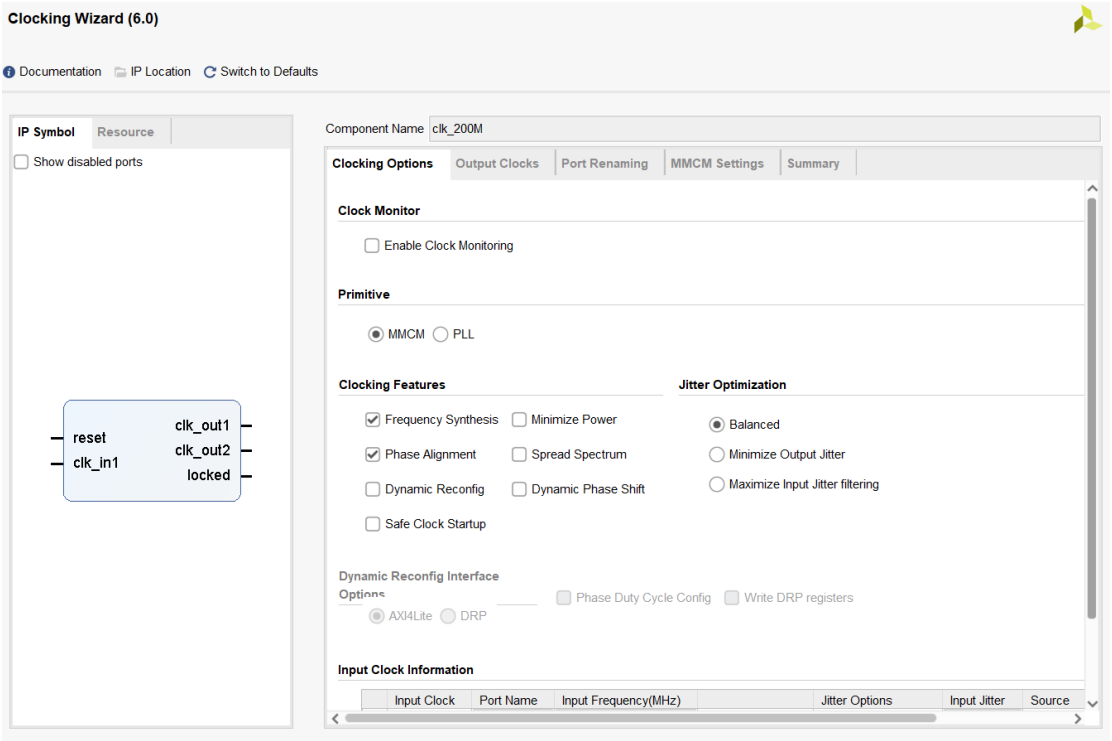

Vivado Project Options:
Target Device : xc7s50-fgga484
Speed Grade : -1
HDL : verilog
Synthesis Tool : VIVADO
If any of the above options are incorrect, please click on "Cancel", change the CORE Gener
MIG Output Options:
Module Name : ddr3
No of Controllers : 1
Selected Compatible Device(s) : --
FPGA Options:
System Clock Type : No Buffer
Reference Clock Type : Use System Clock
Debug Port : OFF
Internal Vref : disabled
IO Power Reduction : ON
XADC instantiation in MIG : Enabled
Extended FPGA Options:
DCI for DQ,DQS/DQS#,DM : enabled
Internal Termination (HR Banks) : 50 Ohms
/***/
/* Controller 0 */
/***/
Controller Options :
Memory : DDR3_SDRAM
Interface : AXI
Design Clock Frequency : 3077 ps (324.99 MHz)
Print
< Back
Next >
Cancel

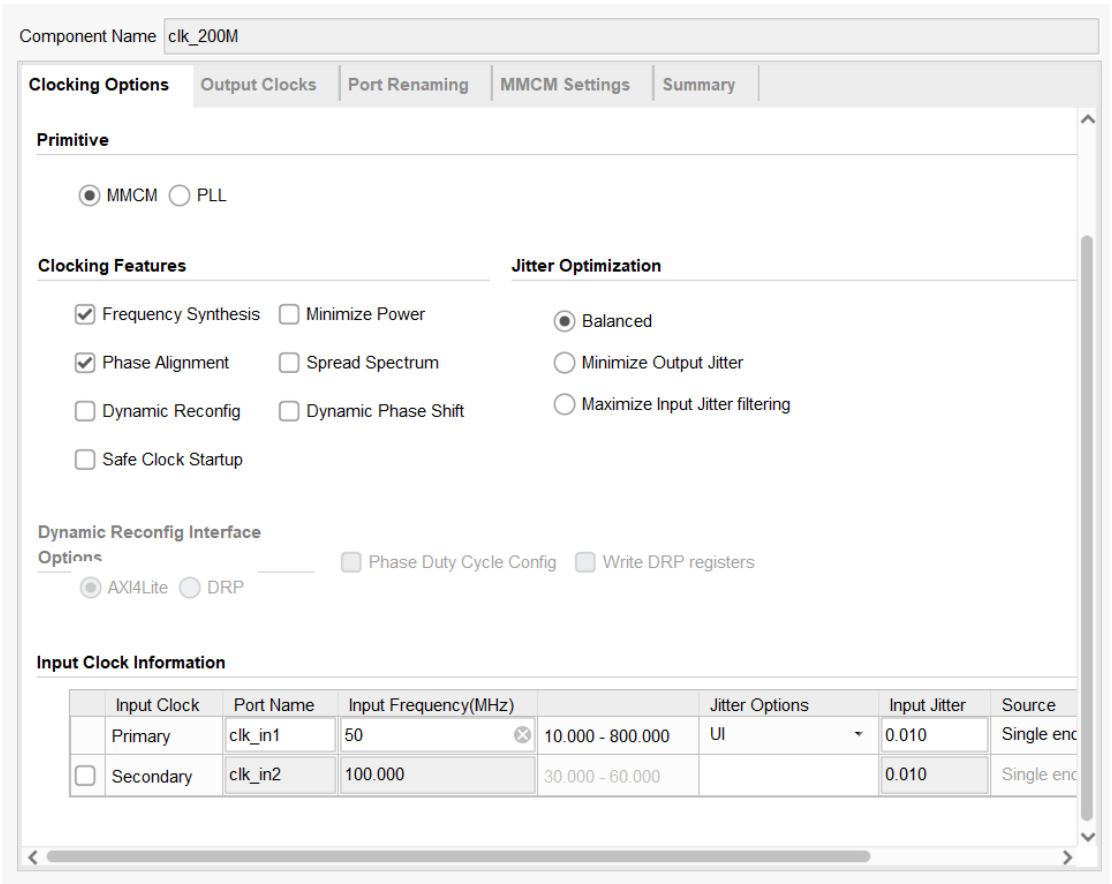
接受协议，下一步：

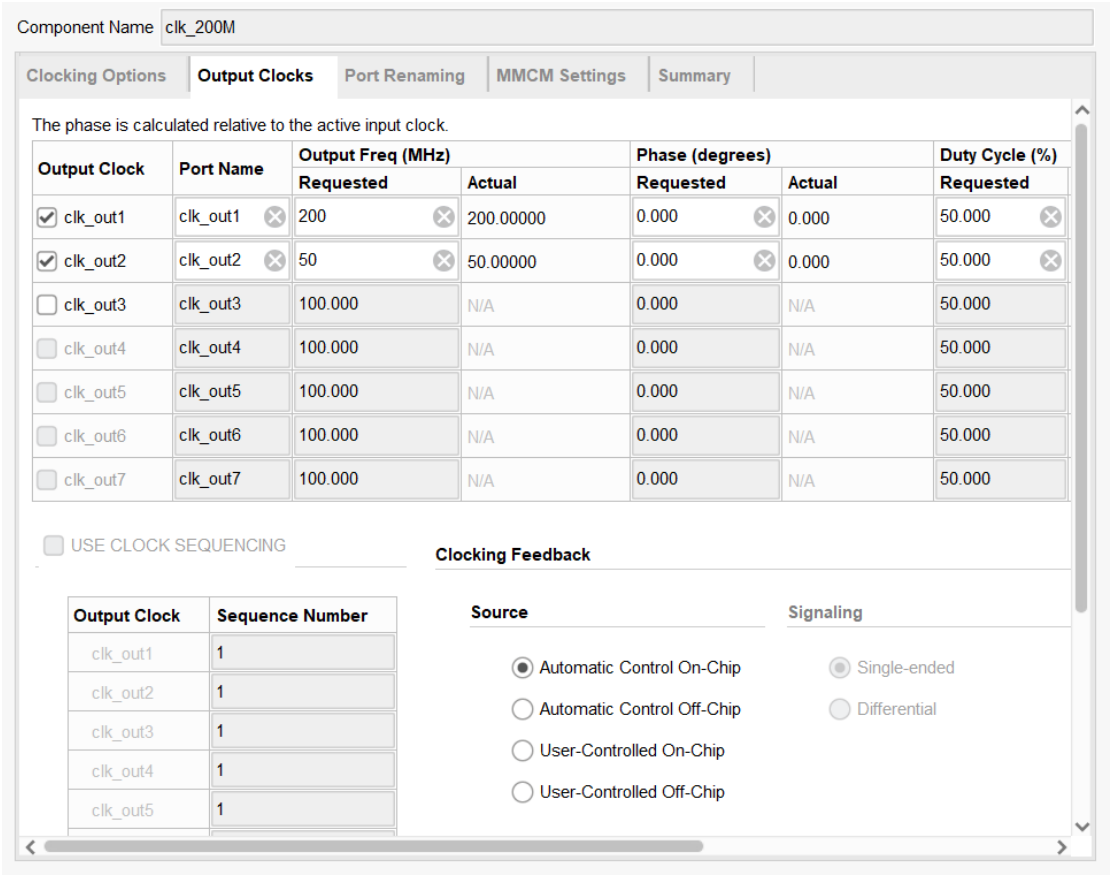


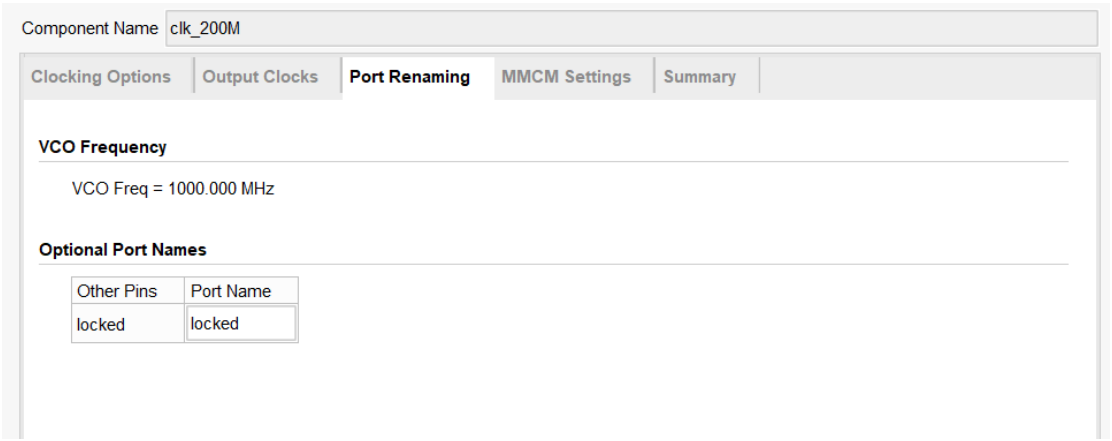
一直下一步直接到 generate，完成 ddr IP 的创建。

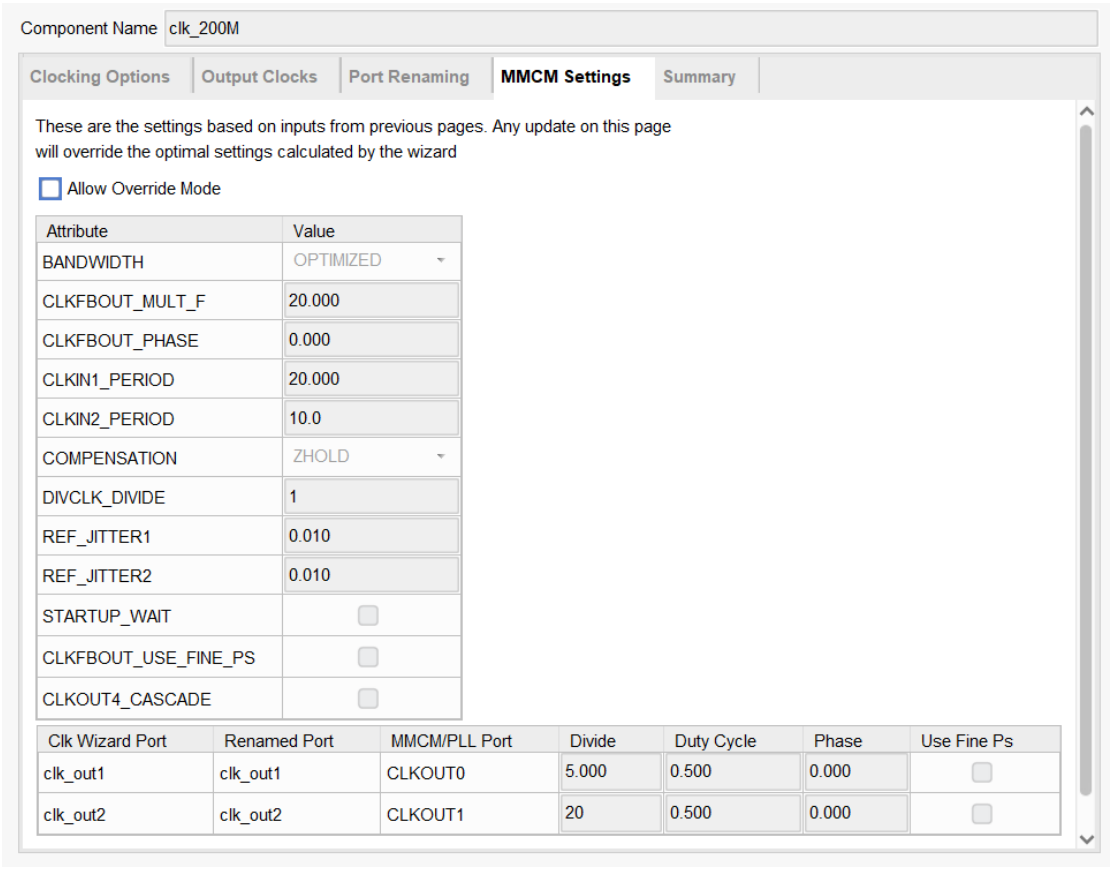
2.5 Clk_200M


Clocking Wizard (6.0)
Documentation
IP Location
Switch to Defaults
IP Symbol
Resource
Show disabled ports
reset
clk_in1
clk_out1
clk_out2
locked
Component Name
clk_200M
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
Clock Monitor
Enable Clock Monitoring
Primitive
MMCM
PLL
Clocking Features
Frequency Synthesis
Minimize Power
Phase Alignment
Spread Spectrum
Dynamic Reconfig
Dynamic Phase Shift
Safe Clock Startup
Jitter Optimization
Balanced
Minimize Output Jitter
Maximize Input Jitter filtering
Dynamic Reconfig Interface Options
AXI4Lite
DRP
Phase Duty Cycle Config
Write DRP registers
Input Clock Information
Input Clock
Port Name
Input Frequency(MHz)
Jitter Options
Input Jitter
Source


Component Name
clk_200M
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
Primitive
MMCM
PLL
Clocking Features
Frequency Synthesis
Minimize Power
Phase Alignment
Spread Spectrum
Dynamic Reconfig
Dynamic Phase Shift
Safe Clock Startup
Jitter Optimization
Balanced
Minimize Output Jitter
Maximize Input Jitter filtering
Dynamic Reconfig Interface Options
AXI4Lite
DRP
Phase Duty Cycle Config
Write DRP registers
Input Clock Information
Input Clock
Port Name
Input Frequency(MHz)
Jitter Options
Input Jitter
Source
Primary
clk_in1
50
10.000 - 800.000
UI
0.010
Single enc
Secondary
clk_in2
100.000
30.000 - 60.000
0.010
Single enc


Component Name clk_200M
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
The phase is calculated relative to the active input clock.
Output Clock
Port Name
Output Freq (MHz)
Requested
Actual
Phase (degrees)
Requested
Actual
Duty Cycle (%)
Requested
clk_out1 clk_out1 200 200.00000 0.000 0.000 50.000
clk_out2 clk_out2 50 50.00000 0.000 0.000 50.000
clk_out3 clk_out3 100.000 N/A 0.000 N/A 50.000
clk_out4 clk_out4 100.000 N/A 0.000 N/A 50.000
clk_out5 clk_out5 100.000 N/A 0.000 N/A 50.000
clk_out6 clk_out6 100.000 N/A 0.000 N/A 50.000
clk_out7 clk_out7 100.000 N/A 0.000 N/A 50.000
USE CLOCK SEQUENCING
Output Clock
Sequence Number
clk_out1 1
clk_out2 1
clk_out3 1
clk_out4 1
clk_out5 1
Clocking Feedback
Source
Automatic Control On-Chip
Automatic Control Off-Chip
User-Controlled On-Chip
User-Controlled Off-Chip
Signaling
Single-ended
Differential


Component Name clk_200M
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
VCO Frequency
VCO Freq = 1000.000 MHz
Optional Port Names
Other Pins
Port Name
locked
locked



Component Name clk_200M

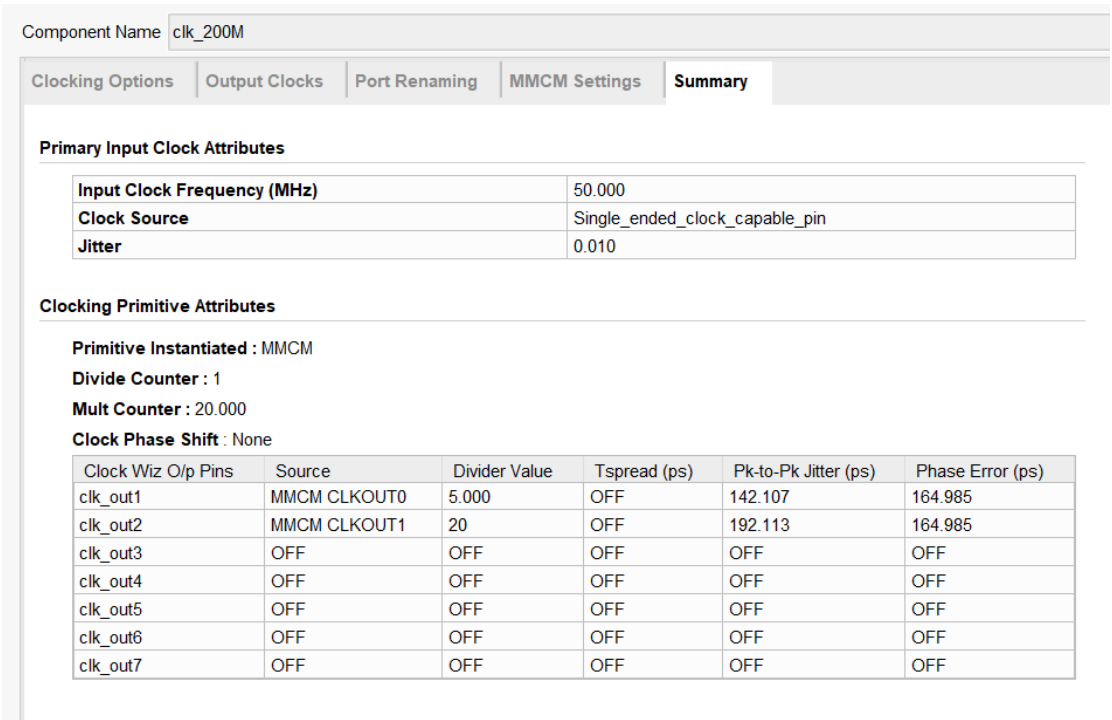
Clocking Options | Output Clocks | Port Renaming | **MMCM Settings** | Summary

These are the settings based on inputs from previous pages. Any update on this page will override the optimal settings calculated by the wizard

Allow Override Mode

Attribute	Value
BANDWIDTH	OPTIMIZED
CLKFBOUT_MULT_F	20.000
CLKFBOUT_PHASE	0.000
CLKIN1_PERIOD	20.000
CLKIN2_PERIOD	10.0
COMPENSATION	ZHOLD
DIVCLK_DIVIDE	1
REF_JITTER1	0.010
REF_JITTER2	0.010
STARTUP_WAIT	
CLKFBOUT_USE_FINE_PS	
CLKOUT4_CASCADE	

Clk Wizard Port	Renamed Port	MMCM/PLL Port	Divide	Duty Cycle	Phase	Use Fine Ps
clk_out1	clk_out1	CLKOUT0	5.000	0.500	0.000	
clk_out2	clk_out2	CLKOUT1	20	0.500	0.000	



Component Name clk_200M

Clocking Options | Output Clocks | Port Renaming | MMCM Settings | **Summary**

Primary Input Clock Attributes

Input Clock Frequency (MHz)	50.000
Clock Source	Single_ended_clock_capable_pin
Jitter	0.010

Clocking Primitive Attributes

Primitive Instantiated : MMCM

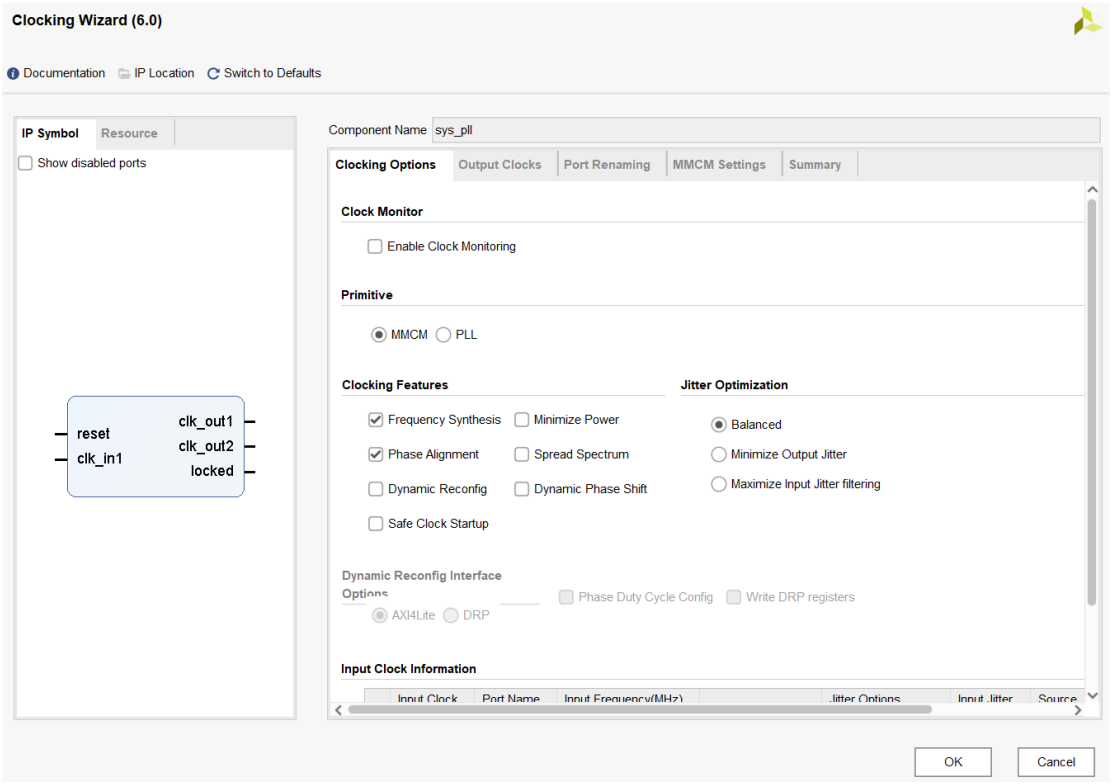
Divide Counter : 1

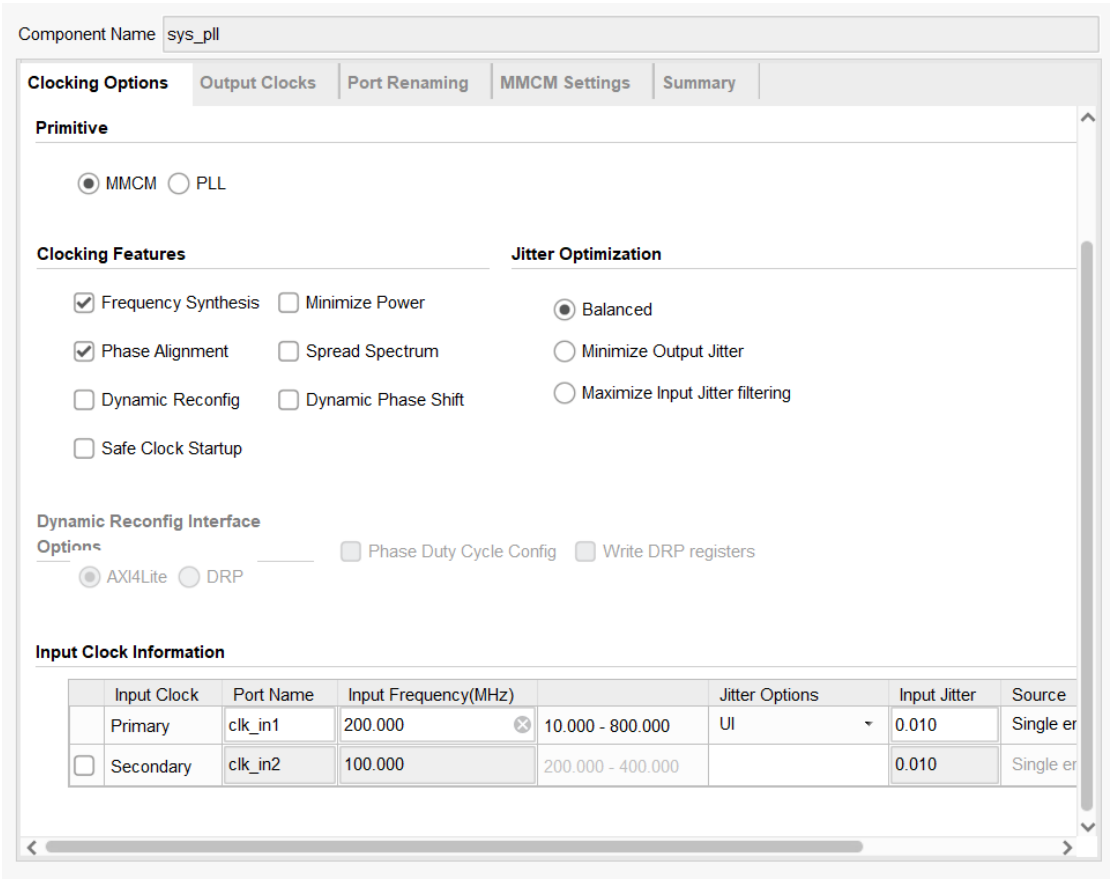
Mult Counter : 20.000

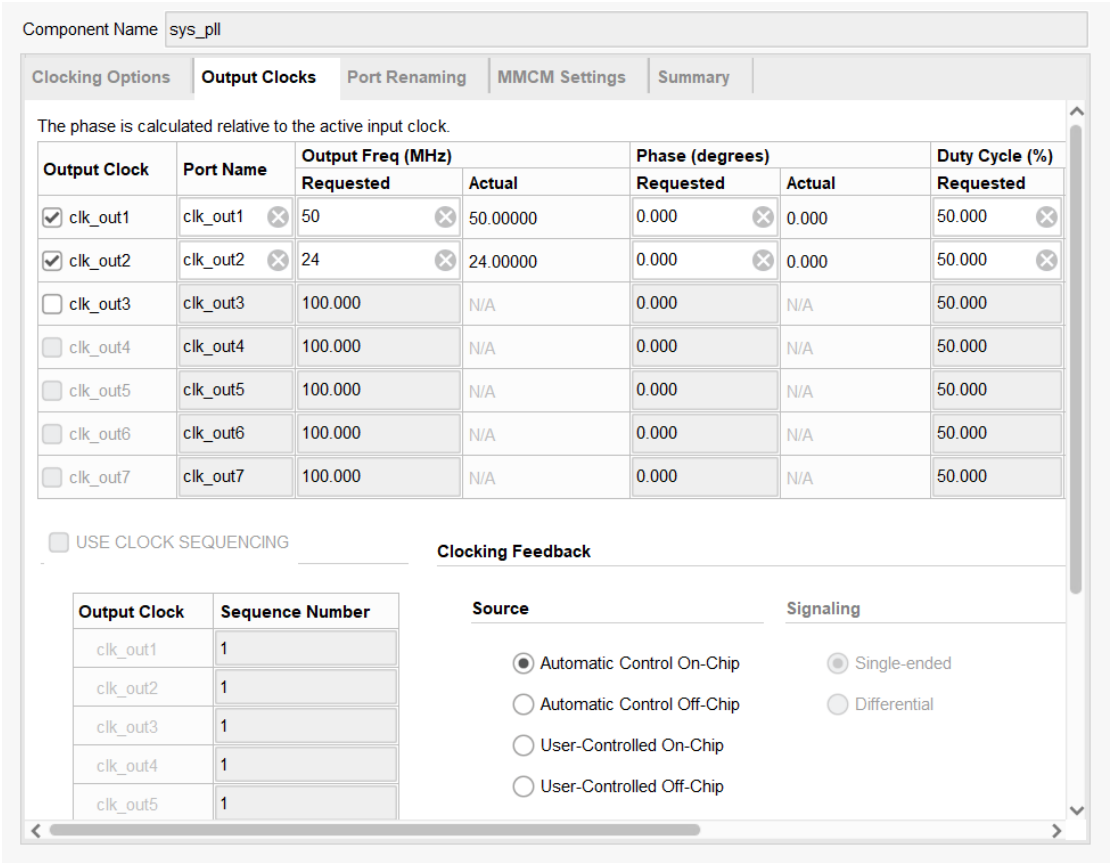
Clock Phase Shift : None

Clock Wiz O/p Pins	Source	Divider Value	Tspread (ps)	Pk-to-Pk Jitter (ps)	Phase Error (ps)
clk_out1	MMCM CLKOUT0	5.000	OFF	142.107	164.985
clk_out2	MMCM CLKOUT1	20	OFF	192.113	164.985
clk_out3	OFF	OFF	OFF	OFF	OFF
clk_out4	OFF	OFF	OFF	OFF	OFF
clk_out5	OFF	OFF	OFF	OFF	OFF
clk_out6	OFF	OFF	OFF	OFF	OFF
clk_out7	OFF	OFF	OFF	OFF	OFF

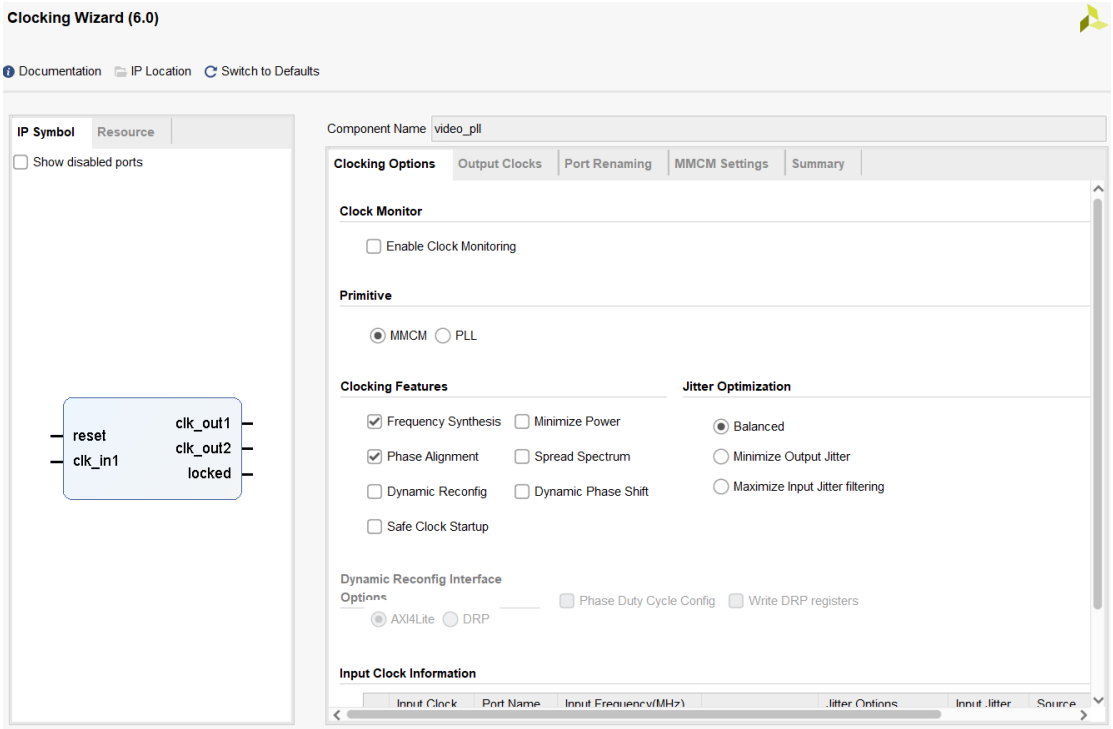
2.6 Sys_pll

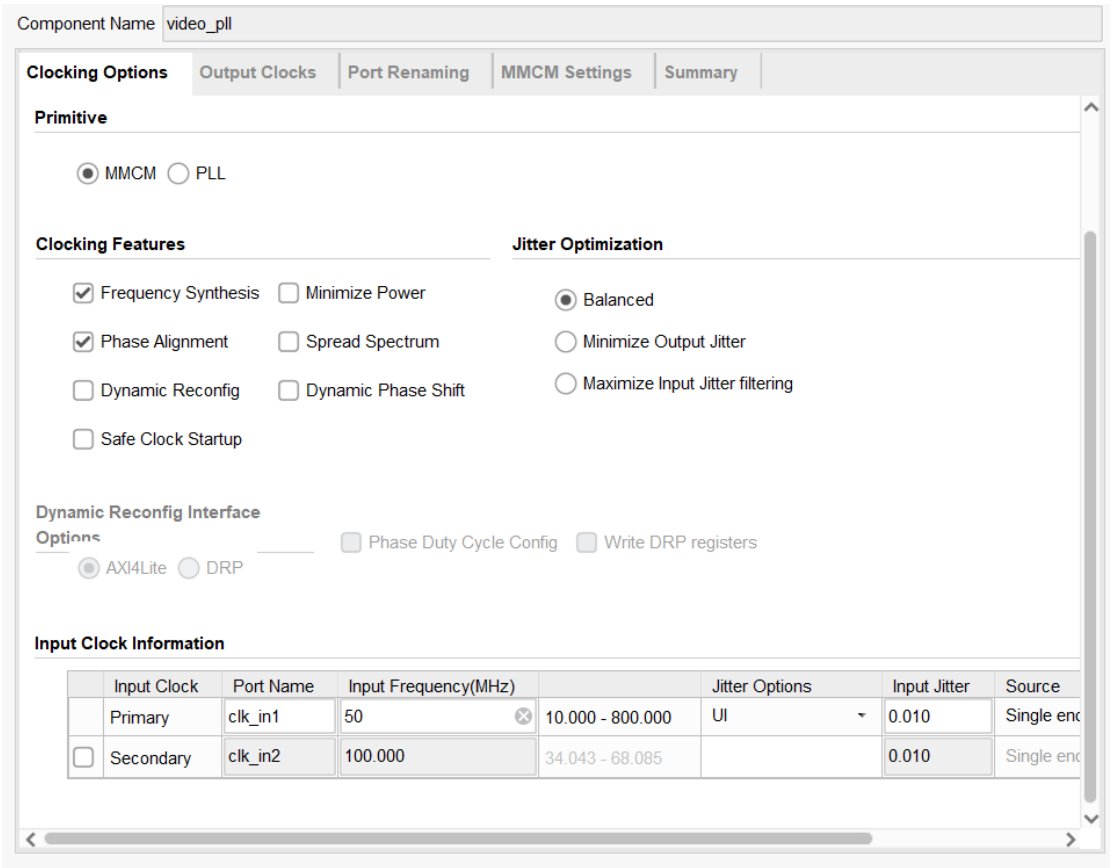

Clocking Wizard (6.0)
Documentation
IP Location
Switch to Defaults
IP Symbol
Resource
Show disabled ports
reset
clk_in1
clk_out1
clk_out2
locked
Component Name
sys_pll
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
Clock Monitor
Enable Clock Monitoring
Primitive
MMCM
PLL
Clocking Features
Frequency Synthesis
Minimize Power
Phase Alignment
Spread Spectrum
Dynamic Reconfig
Dynamic Phase Shift
Safe Clock Startup
Jitter Optimization
Balanced
Minimize Output Jitter
Maximize Input Jitter filtering
Dynamic Reconfig Interface Options
AXI4Lite
DRP
Phase Duty Cycle Config
Write DRP registers
Input Clock Information
OK
Cancel

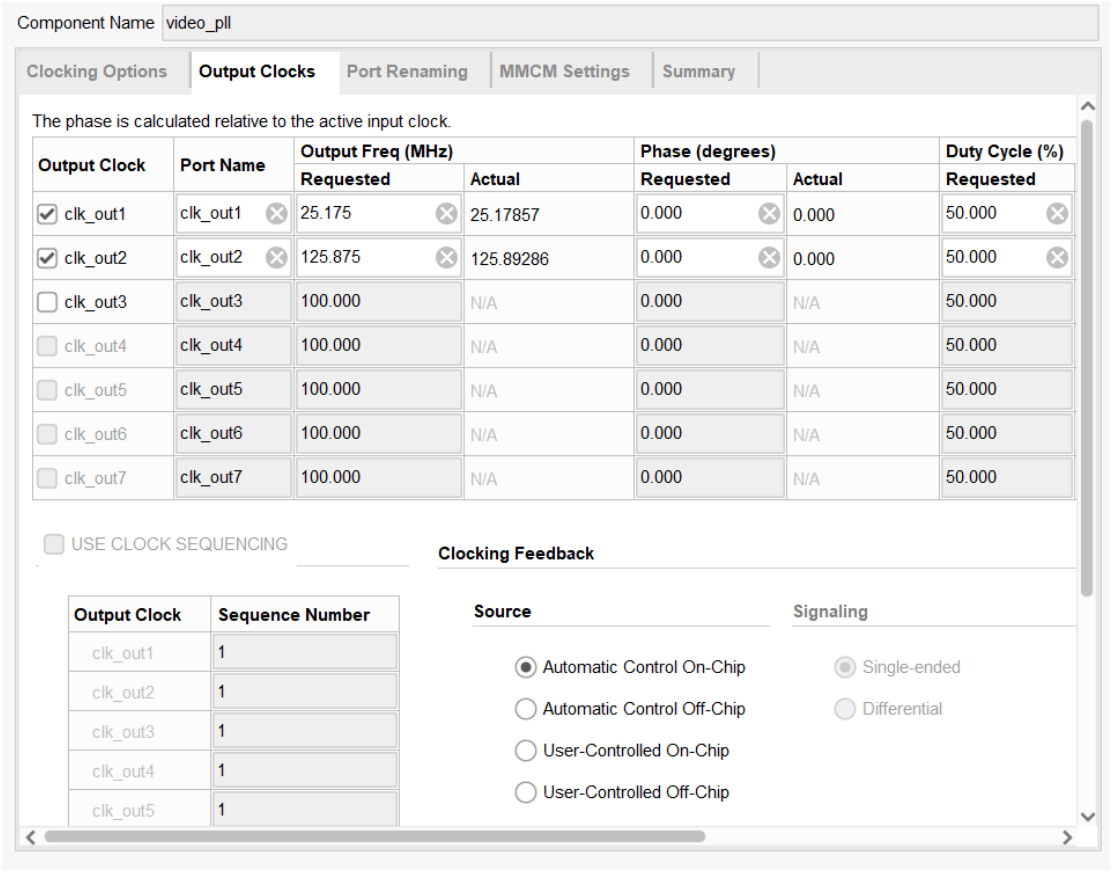

Component Name sys_pll
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
Primitive
MMCM
PLL
Clocking Features
Frequency Synthesis
Minimize Power
Phase Alignment
Spread Spectrum
Dynamic Reconfig
Dynamic Phase Shift
Safe Clock Startup
Jitter Optimization
Balanced
Minimize Output Jitter
Maximize Input Jitter filtering
Dynamic Reconfig Interface Options
AXI4Lite
DRP
Phase Duty Cycle Config
Write DRP registers
Input Clock Information
Input Clock
Port Name
Input Frequency(MHz)
Jitter Options
Input Jitter
Source
Primary
clk_in1
200.000
10.000 - 800.000
UI
0.010
Single er
Secondary
clk_in2
100.000
200.000 - 400.000
0.010
Single er


Component Name sys_pll
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
The phase is calculated relative to the active input clock.
Output Clock
Port Name
Output Freq (MHz)
Requested
Actual
Phase (degrees)
Requested
Actual
Duty Cycle (%)
Requested
clk_out1
clk_out1
50
50.00000
0.000
0.000
50.000
clk_out2
clk_out2
24
24.00000
0.000
0.000
50.000
clk_out3
clk_out3
100.000
N/A
0.000
N/A
50.000
clk_out4
clk_out4
100.000
N/A
0.000
N/A
50.000
clk_out5
clk_out5
100.000
N/A
0.000
N/A
50.000
clk_out6
clk_out6
100.000
N/A
0.000
N/A
50.000
clk_out7
clk_out7
100.000
N/A
0.000
N/A
50.000
USE CLOCK SEQUENCING
Output Clock
Sequence Number
clk_out1
1
clk_out2
1
clk_out3
1
clk_out4
1
clk_out5
1
Clocking Feedback
Source
Automatic Control On-Chip
Automatic Control Off-Chip
User-Controlled On-Chip
User-Controlled Off-Chip
Signaling
Single-ended
Differential

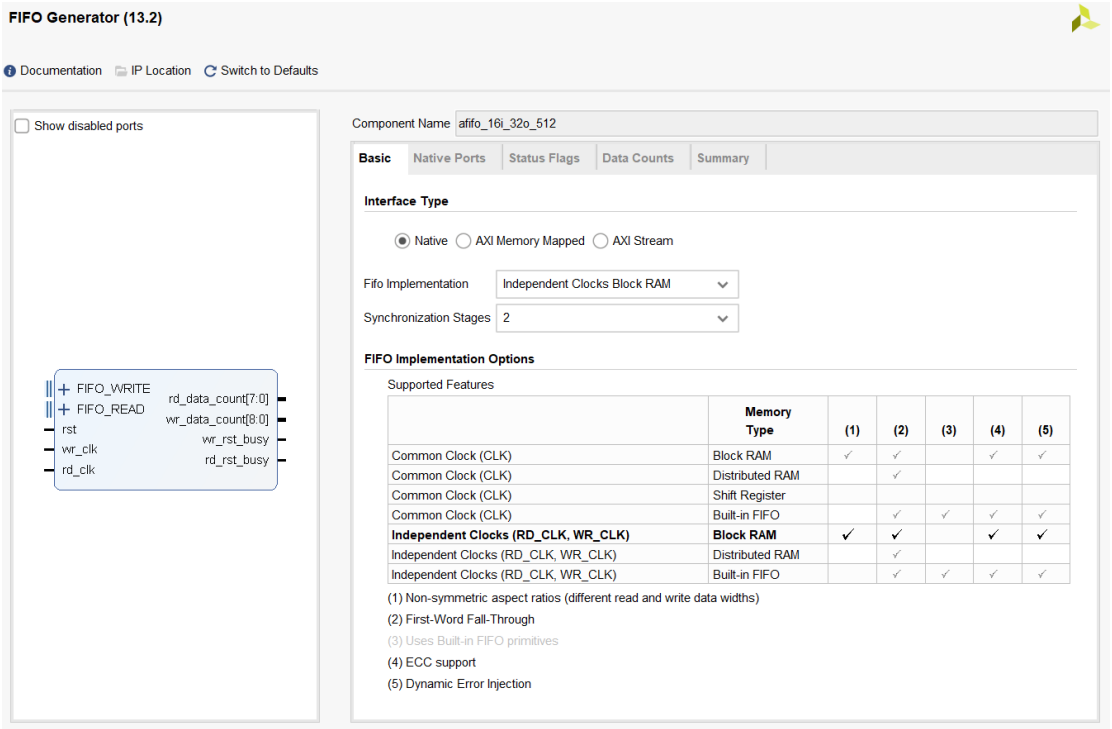
2.7 Video_pll

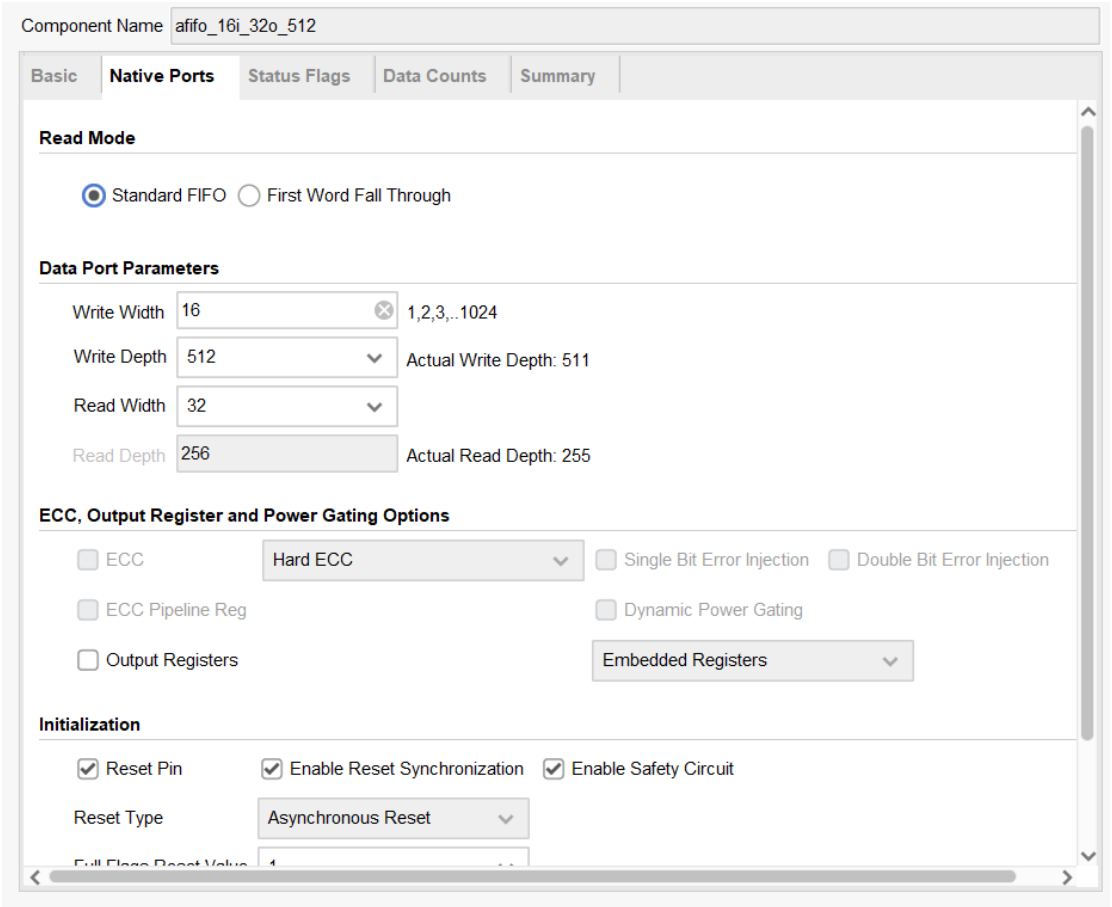

Clocking Wizard (6.0)
Documentation
IP Location
Switch to Defaults
IP Symbol
Resource
Show disabled ports
reset
clk_in1
clk_out1
clk_out2
locked
Component Name
video_pll
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
Clock Monitor
Enable Clock Monitoring
Primitive
MMCM
PLL
Clocking Features
Frequency Synthesis
Minimize Power
Phase Alignment
Spread Spectrum
Dynamic Reconfig
Dynamic Phase Shift
Safe Clock Startup
Jitter Optimization
Balanced
Minimize Output Jitter
Maximize Input Jitter filtering
Dynamic Reconfig Interface Options
AXI4Lite
DRP
Phase Duty Cycle Config
Write DRP registers
Input Clock Information

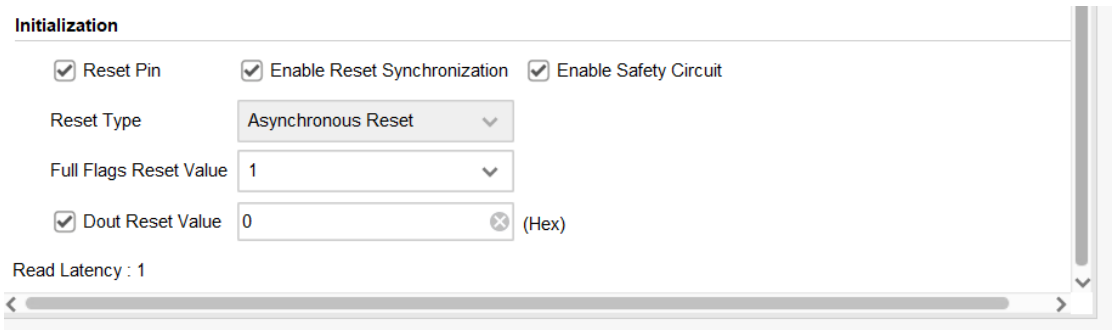

Component Name
video_pll
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
Primitive
MMCM
PLL
Clocking Features
Frequency Synthesis
Minimize Power
Phase Alignment
Spread Spectrum
Dynamic Reconfig
Dynamic Phase Shift
Safe Clock Startup
Jitter Optimization
Balanced
Minimize Output Jitter
Maximize Input Jitter filtering
Dynamic Reconfig Interface Options
AXI4Lite
DRP
Phase Duty Cycle Config
Write DRP registers
Input Clock Information
Input Clock
Port Name
Input Frequency(MHz)
Jitter Options
Input Jitter
Source
Primary
clk_in1
50
10.000 - 800.000
UI
0.010
Single enc
Secondary
clk_in2
100.000
34.043 - 68.085
0.010
Single enc

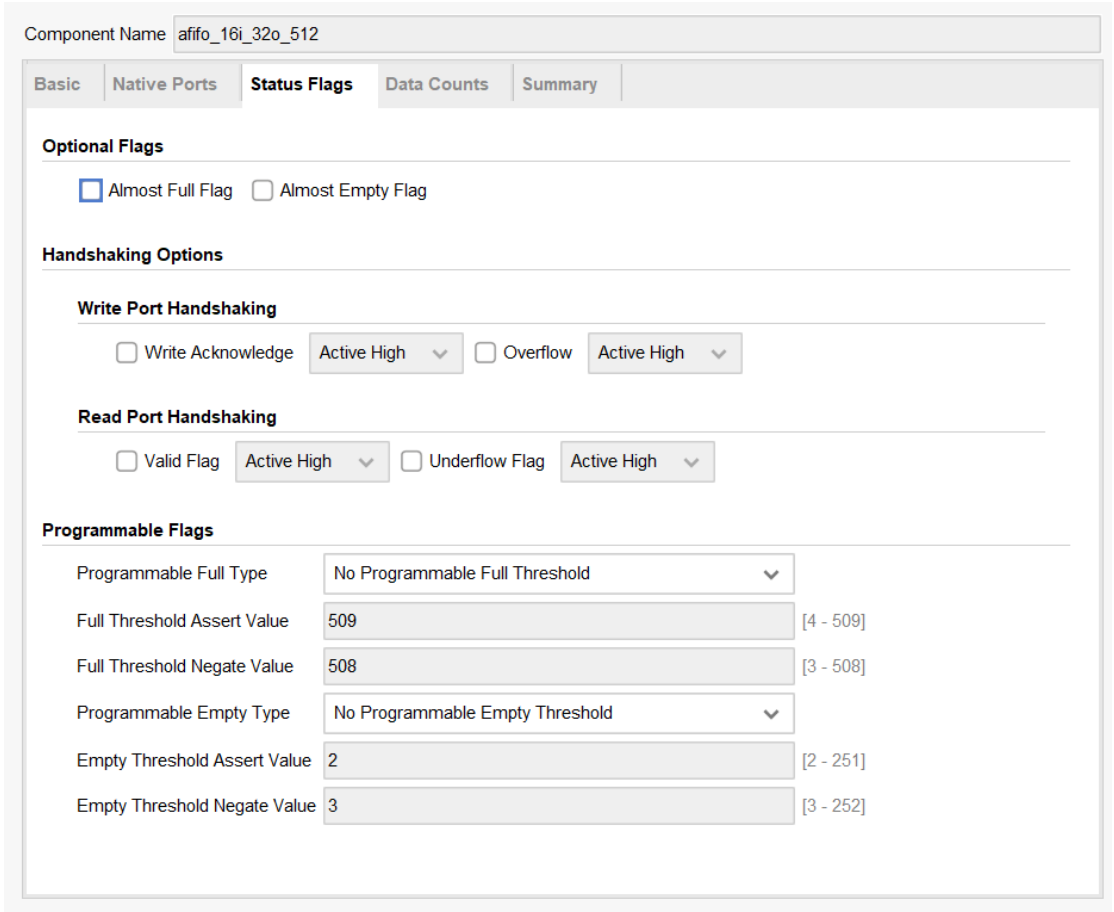

Component Name
video_pll
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
The phase is calculated relative to the active input clock.
Output Clock
Port Name
Output Freq (MHz)
Requested
Actual
Phase (degrees)
Requested
Actual
Duty Cycle (%)
Requested
clk_out1 clk_out1 25.175 25.17857 0.000 0.000 50.000
clk_out2 clk_out2 125.875 125.89286 0.000 0.000 50.000
clk_out3 clk_out3 100.000 N/A 0.000 N/A 50.000
clk_out4 clk_out4 100.000 N/A 0.000 N/A 50.000
clk_out5 clk_out5 100.000 N/A 0.000 N/A 50.000
clk_out6 clk_out6 100.000 N/A 0.000 N/A 50.000
clk_out7 clk_out7 100.000 N/A 0.000 N/A 50.000
USE CLOCK SEQUENCING
Output Clock
Sequence Number
clk_out1 1
clk_out2 1
clk_out3 1
clk_out4 1
clk_out5 1
Clocking Feedback
Source
Automatic Control On-Chip
Automatic Control Off-Chip
User-Controlled On-Chip
User-Controlled Off-Chip
Signaling
Single-ended
Differential

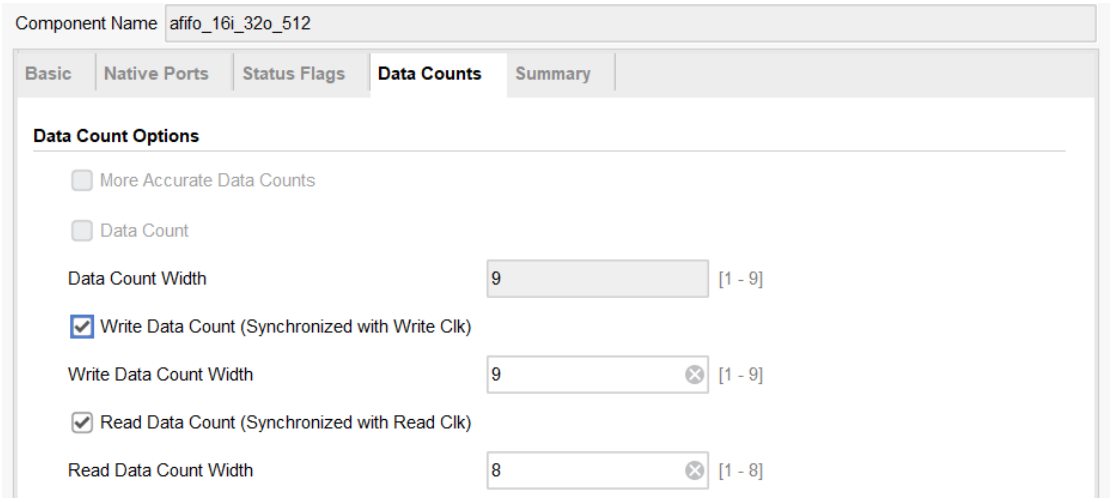
2.8 Write fifo

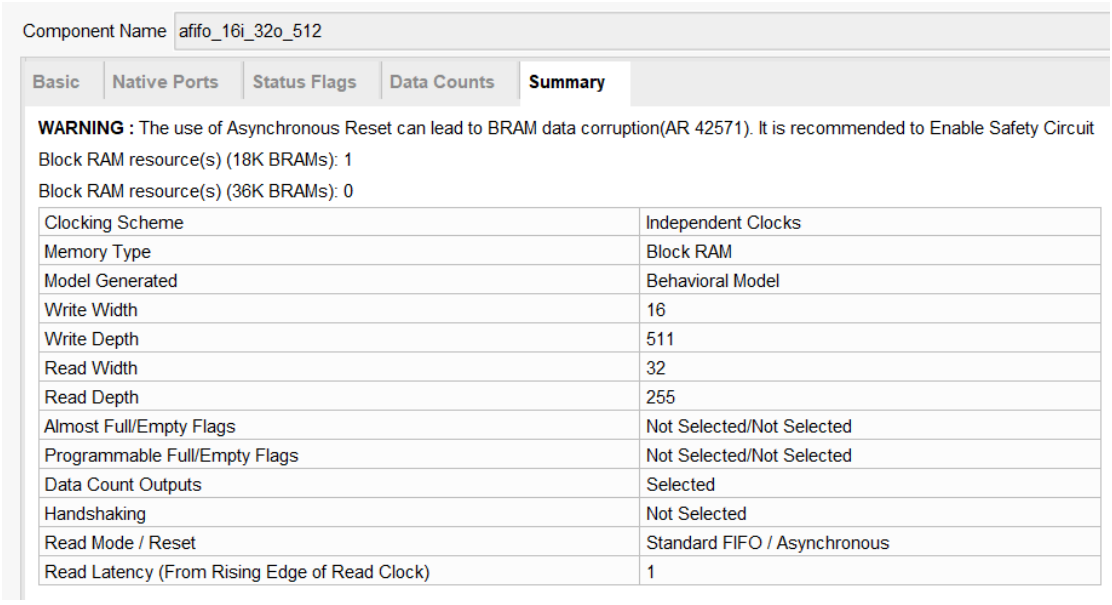




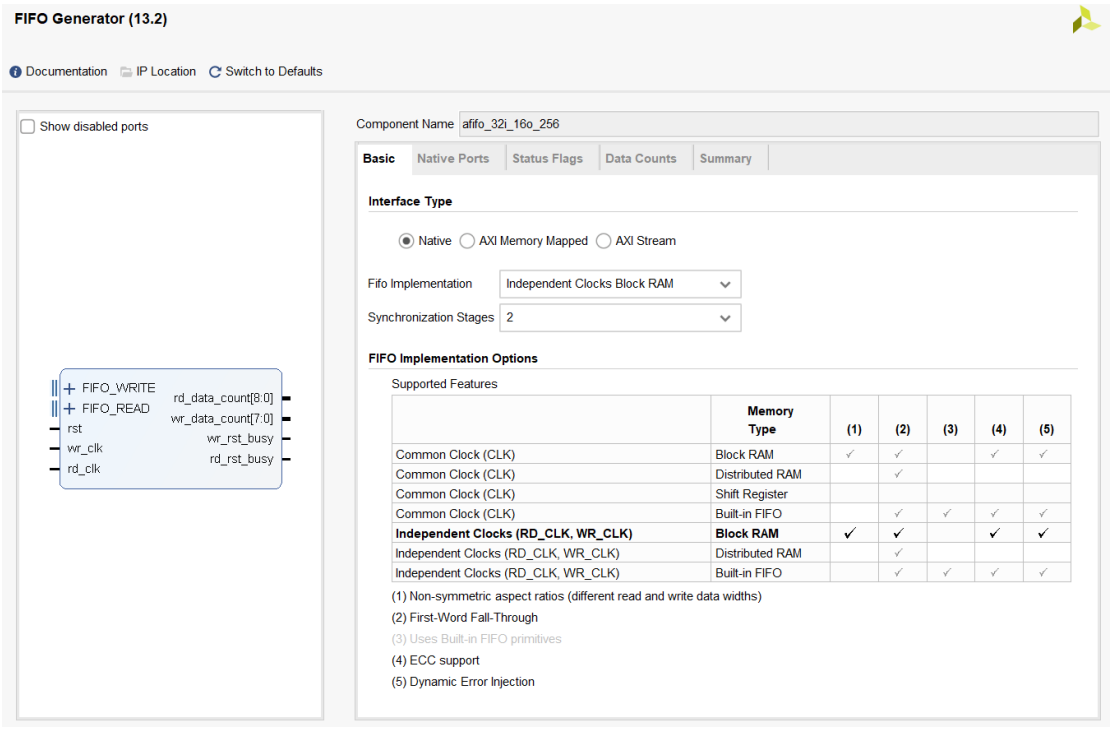

Initialization
Reset Pin
Enable Reset Synchronization
Enable Safety Circuit
Reset Type
Asynchronous Reset
Full Flags Reset Value
1
Dout Reset Value
0
(Hex)
Read Latency : 1

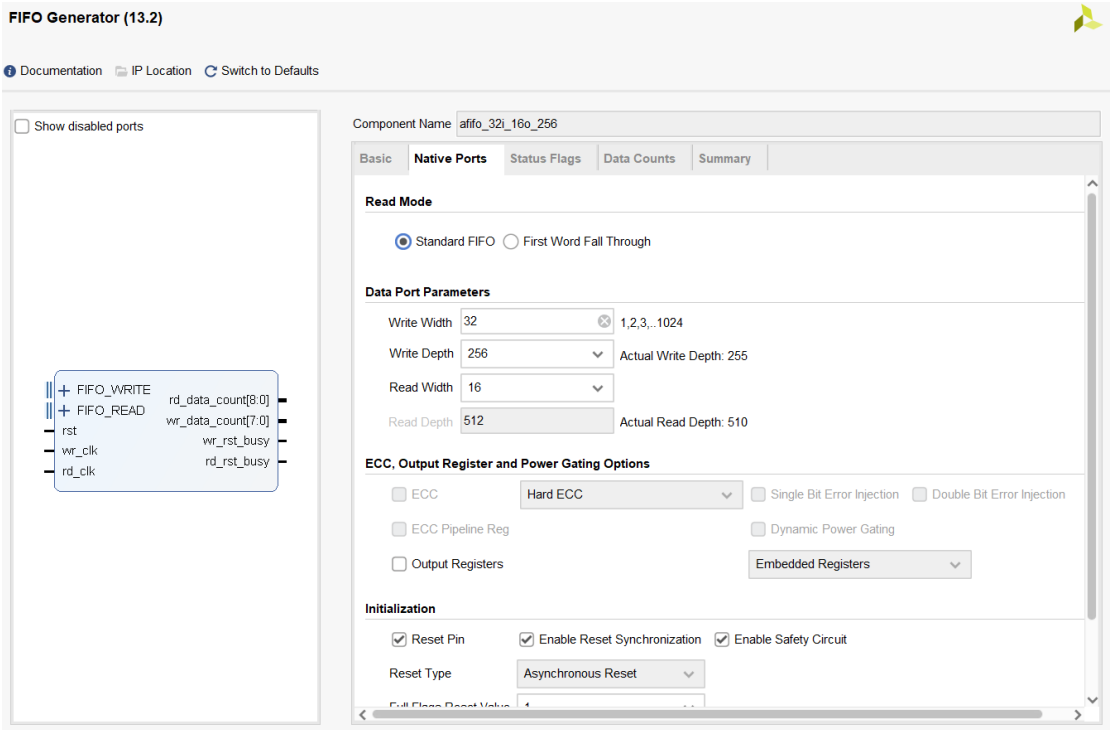

Component Name
afifo_16i_32o_512
Basic
Native Ports
Status Flags
Data Counts
Summary
Optional Flags
Almost Full Flag
Almost Empty Flag
Handshaking Options
Write Port Handshaking
Write Acknowledge
Active High
Overflow
Active High
Read Port Handshaking
Valid Flag
Active High
Underflow Flag
Active High
Programmable Flags
Programmable Full Type
No Programmable Full Threshold
Full Threshold Assert Value
509
[4 - 509]
Full Threshold Negate Value
508
[3 - 508]
Programmable Empty Type
No Programmable Empty Threshold
Empty Threshold Assert Value
2
[2 - 251]
Empty Threshold Negate Value
3
[3 - 252]

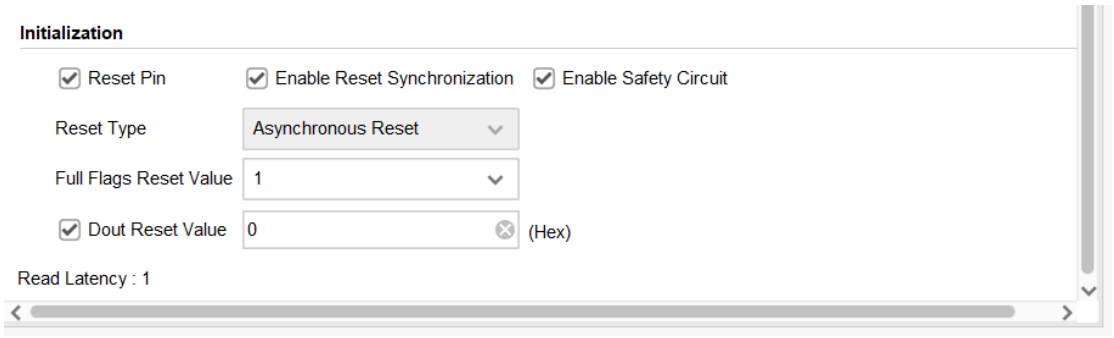

Component Name
afifo_16i_32o_512
Basic
Native Ports
Status Flags
Data Counts
Summary
Data Count Options
More Accurate Data Counts
Data Count
Data Count Width
9
[1 - 9]
Write Data Count (Synchronized with Write Clk)
Write Data Count Width
9
[1 - 9]
Read Data Count (Synchronized with Read Clk)
Read Data Count Width
8
[1 - 8]

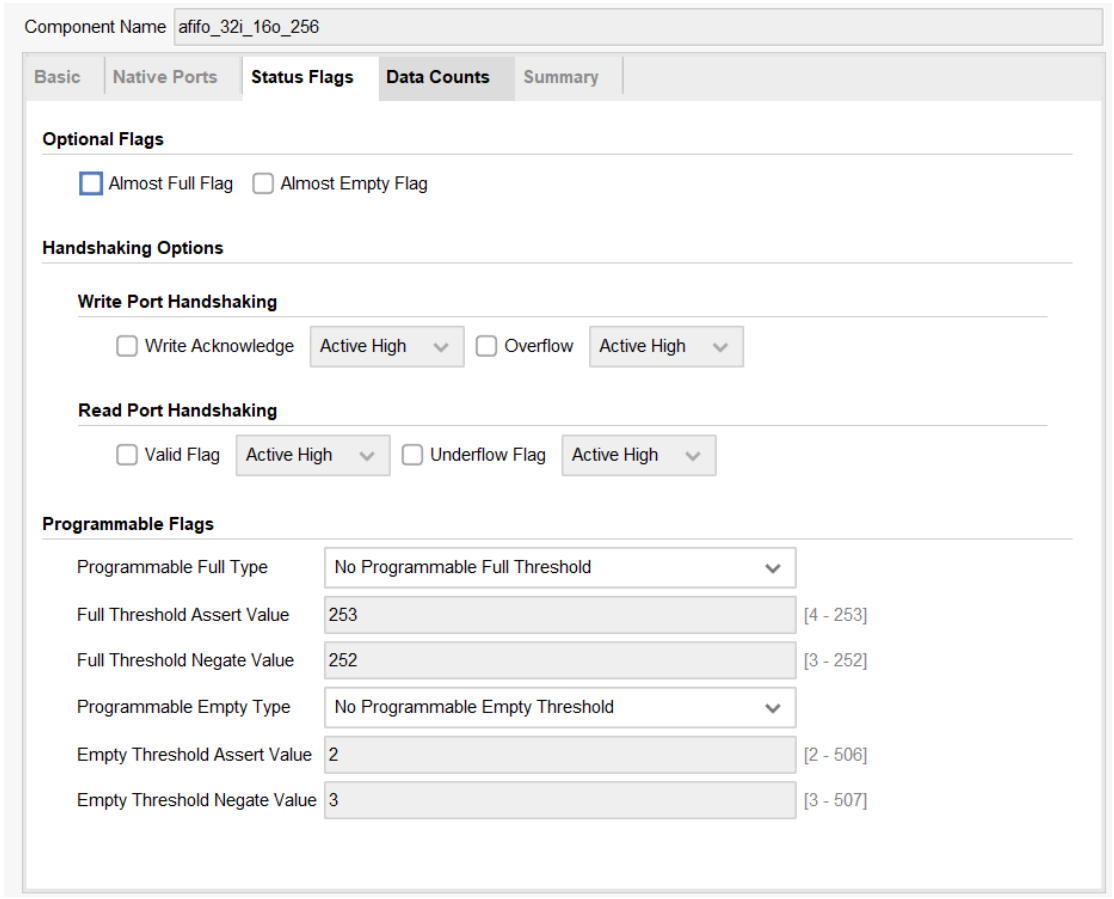

Component Name
afifo_16i_32o_512
Basic
Native Ports
Status Flags
Data Counts
Summary
WARNING : The use of Asynchronous Reset can lead to BRAM data corruption(AR 42571). It is recommended to Enable Safety Circuit
Block RAM resource(s) (18K BRAMs): 1
Block RAM resource(s) (36K BRAMs): 0
Clocking Scheme
Independent Clocks
Memory Type
Block RAM
Model Generated
Behavioral Model
Write Width
16
Write Depth
511
Read Width
32
Read Depth
255
Almost Full/Empty Flags
Not Selected/Not Selected
Programmable Full/Empty Flags
Not Selected/Not Selected
Data Count Outputs
Selected
Handshaking
Not Selected
Read Mode / Reset
Standard FIFO / Asynchronous
Read Latency (From Rising Edge of Read Clock)
1

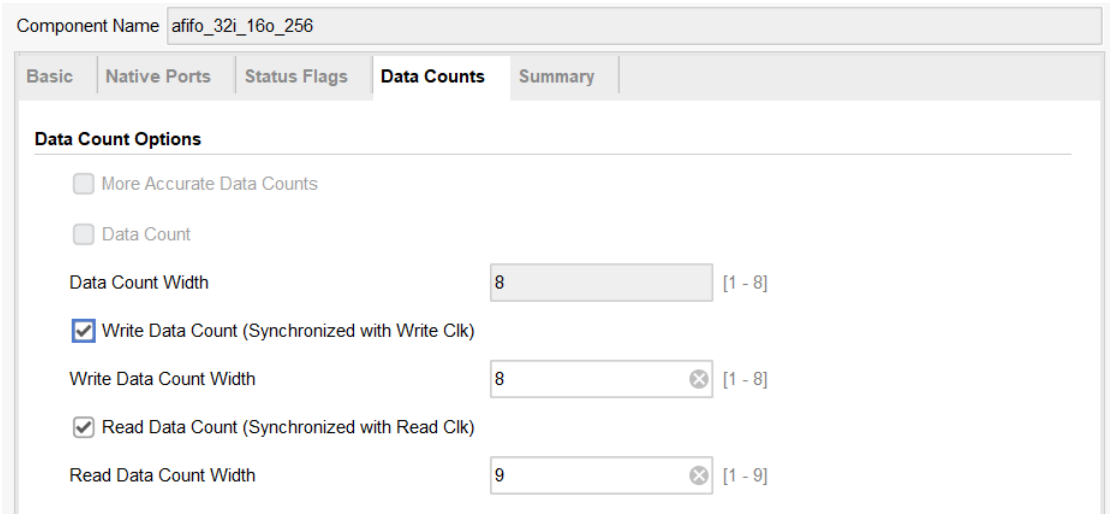
2.9 Read fifo

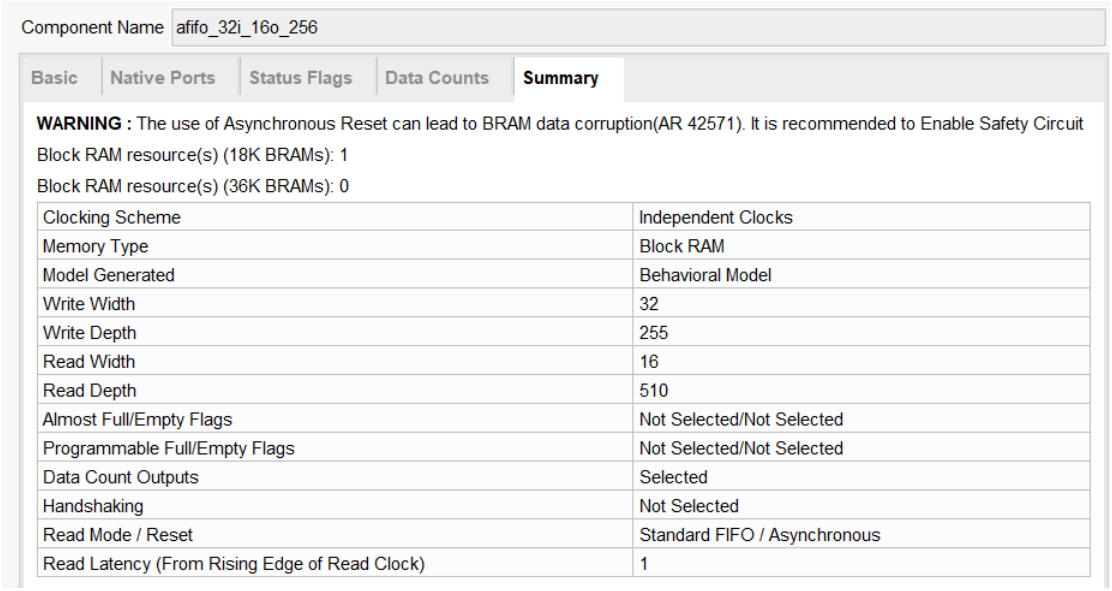

FIFO Generator (13.2)
Documentation
IP Location
Switch to Defaults
Show disabled ports
FIFO_WRITE
FIFO_READ
rst
wr_clk
rd_clk
rd_data_count[8:0]
wr_data_count[7:0]
wr_rst_busy
rd_rst_busy
Component Name
afifo_32i_16o_256
Basic
Native Ports
Status Flags
Data Counts
Summary
Interface Type
Native
AXI Memory Mapped
AXI Stream
Fifo Implementation
Independent Clocks Block RAM
Synchronization Stages
2
FIFO Implementation Options
Supported Features
Memory Type
(1)
(2)
(3)
(4)
(5)
Common Clock (CLK) Block RAM
Common Clock (CLK) Distributed RAM
Common Clock (CLK) Shift Register
Common Clock (CLK) Built-in FIFO
Independent Clocks (RD_CLK, WR_CLK) Block RAM
Independent Clocks (RD_CLK, WR_CLK) Distributed RAM
Independent Clocks (RD_CLK, WR_CLK) Built-in FIFO
(1) Non-symmetric aspect ratios (different read and write data widths)
(2) First-Word Fall-Through
(3) Uses Built-in FIFO primitives
(4) ECC support
(5) Dynamic Error Injection


FIFO Generator (13.2)
Documentation
IP Location
Switch to Defaults
Show disabled ports
FIFO_WRITE
FIFO_READ
rst
wr_clk
rd_clk
rd_data_count[8:0]
wr_data_count[7:0]
wr_rst_busy
rd_rst_busy
Component Name
afifo_32i_16o_256
Basic
Native Ports
Status Flags
Data Counts
Summary
Read Mode
Standard FIFO
First Word Fall Through
Data Port Parameters
Write Width
32
1,2,3,..1024
Write Depth
256
Actual Write Depth: 255
Read Width
16
Read Depth
512
Actual Read Depth: 510
ECC, Output Register and Power Gating Options
ECC
Hard ECC
Single Bit Error Injection
Double Bit Error Injection
ECC Pipeline Reg
Dynamic Power Gating
Output Registers
Embedded Registers
Initialization
Reset Pin
Enable Reset Synchronization
Enable Safety Circuit
Reset Type
Asynchronous Reset

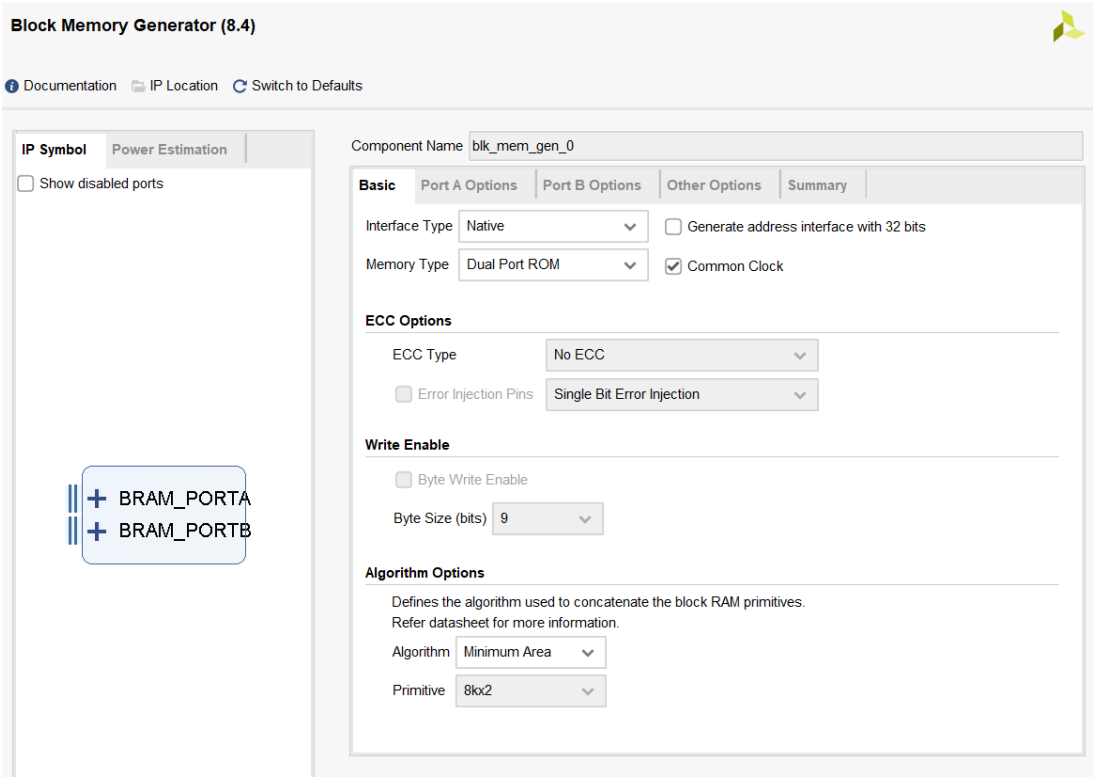

Initialization
Reset Pin
Enable Reset Synchronization
Enable Safety Circuit
Reset Type
Asynchronous Reset
Full Flags Reset Value
1
Dout Reset Value
0
(Hex)
Read Latency : 1

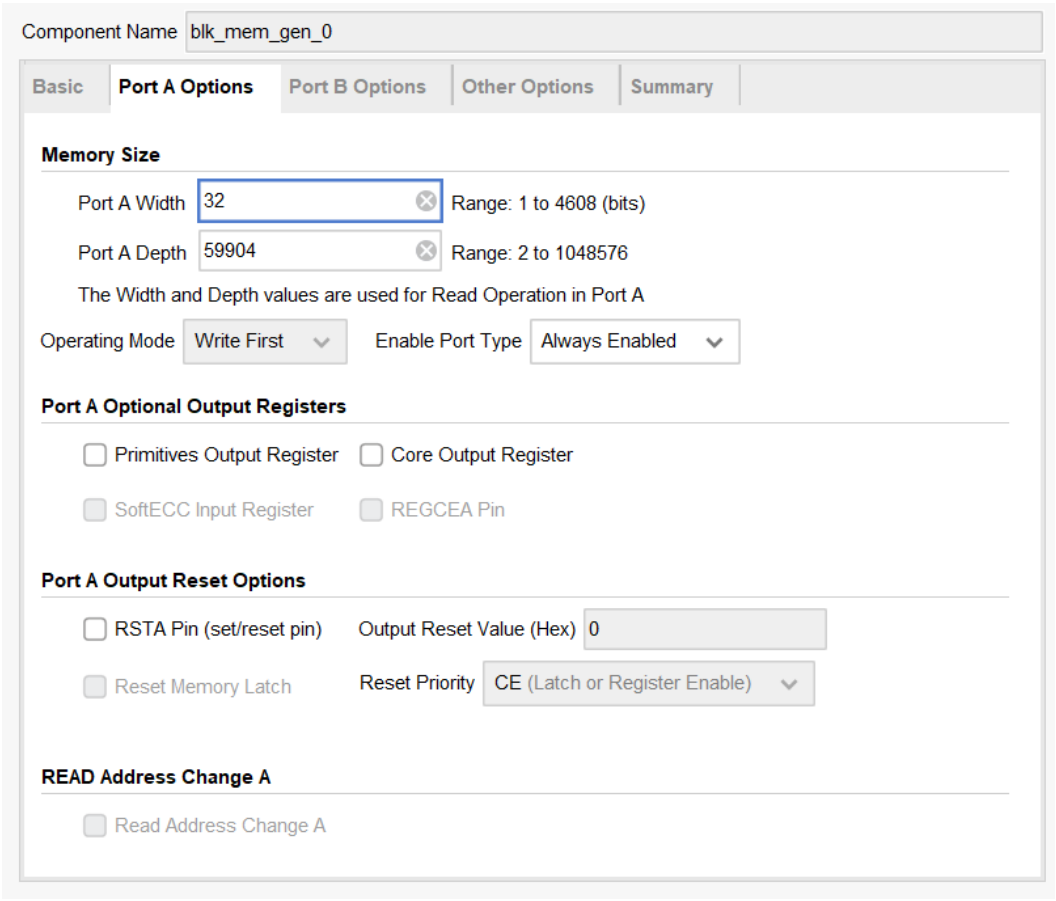

Component Name
afifo_32i_16o_256
Basic
Native Ports
Status Flags
Data Counts
Summary
Optional Flags
Almost Full Flag
Almost Empty Flag
Handshaking Options
Write Port Handshaking
Write Acknowledge
Active High
Overflow
Active High
Read Port Handshaking
Valid Flag
Active High
Underflow Flag
Active High
Programmable Flags
Programmable Full Type
No Programmable Full Threshold
Full Threshold Assert Value
253
[4 - 253]
Full Threshold Negate Value
252
[3 - 252]
Programmable Empty Type
No Programmable Empty Threshold
Empty Threshold Assert Value
2
[2 - 506]
Empty Threshold Negate Value
3
[3 - 507]

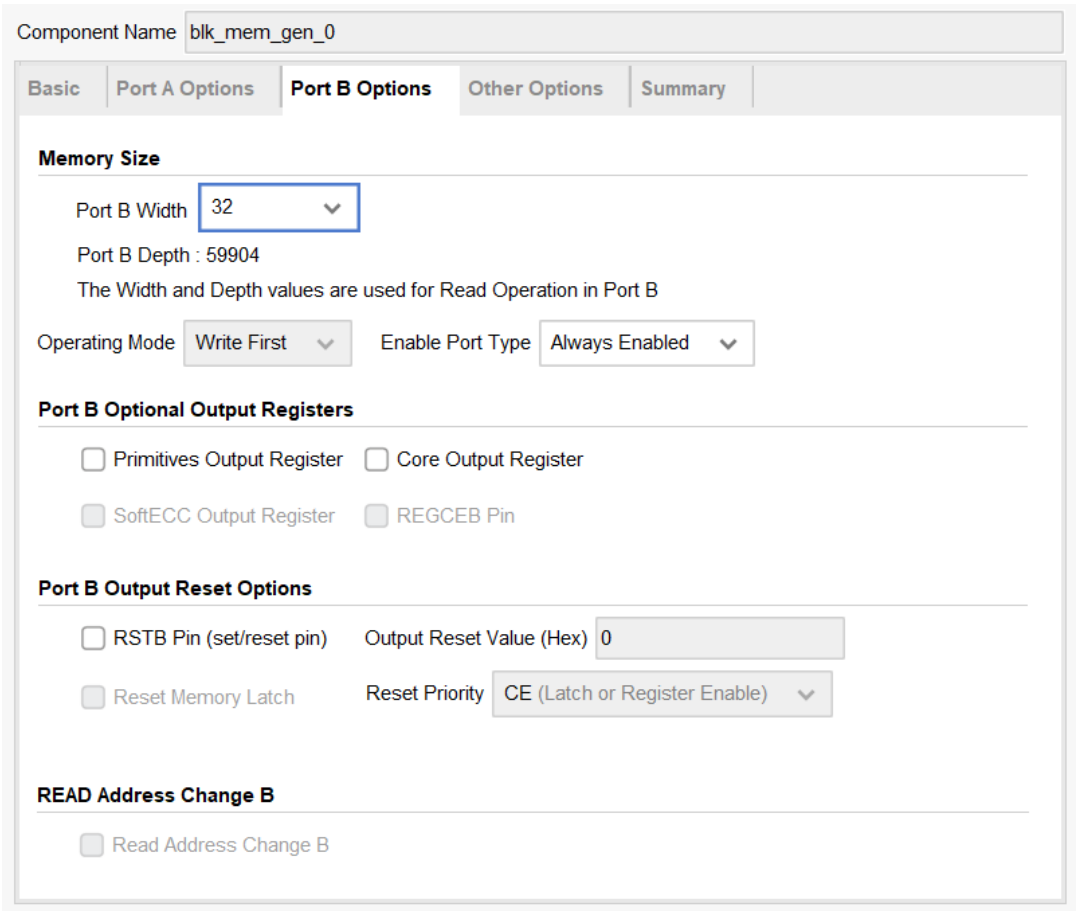

Component Name afifo_32i_16o_256
Basic
Native Ports
Status Flags
Data Counts
Summary
Data Count Options
More Accurate Data Counts
Data Count
Data Count Width
8
[1 - 8]
Write Data Count (Synchronized with Write Clk)
Write Data Count Width
8
[1 - 8]
Read Data Count (Synchronized with Read Clk)
Read Data Count Width
9
[1 - 9]

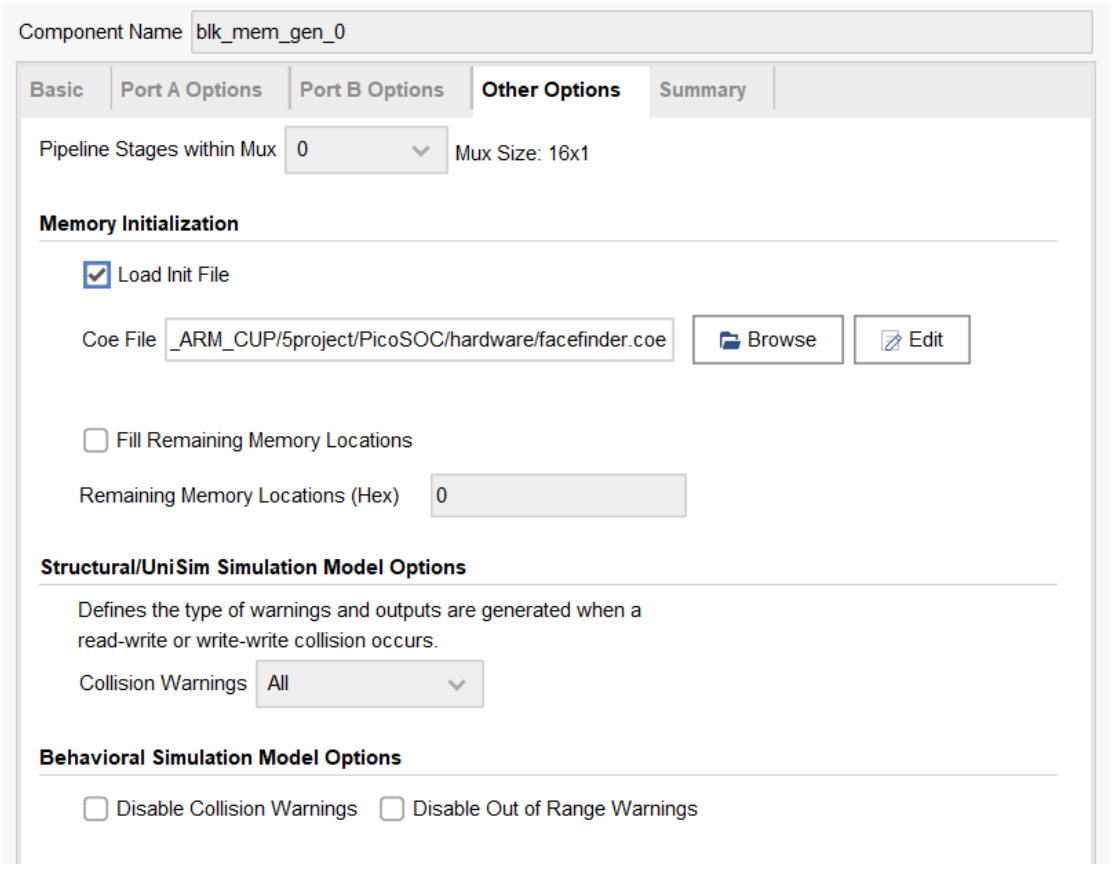

Component Name afifo_32i_16o_256
Basic
Native Ports
Status Flags
Data Counts
Summary
WARNING : The use of Asynchronous Reset can lead to BRAM data corruption(AR 42571). It is recommended to Enable Safety Circuit
Block RAM resource(s) (18K BRAMs): 1
Block RAM resource(s) (36K BRAMs): 0
Clocking Scheme
Independent Clocks
Memory Type
Block RAM
Model Generated
Behavioral Model
Write Width
32
Write Depth
255
Read Width
16
Read Depth
510
Almost Full/Empty Flags
Not Selected/Not Selected
Programmable Full/Empty Flags
Not Selected/Not Selected
Data Count Outputs
Selected
Handshaking
Not Selected
Read Mode / Reset
Standard FIFO / Asynchronous
Read Latency (From Rising Edge of Read Clock)
1

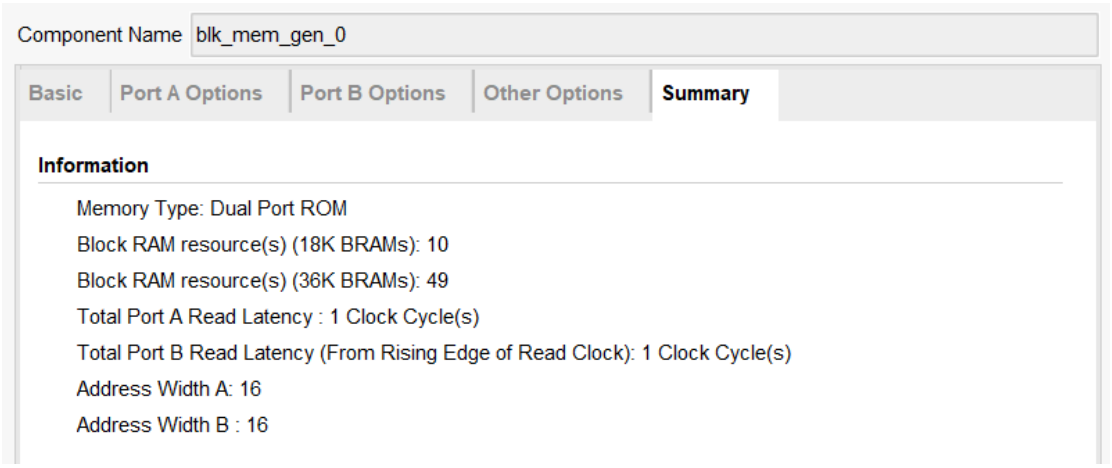
2.10 Block memory



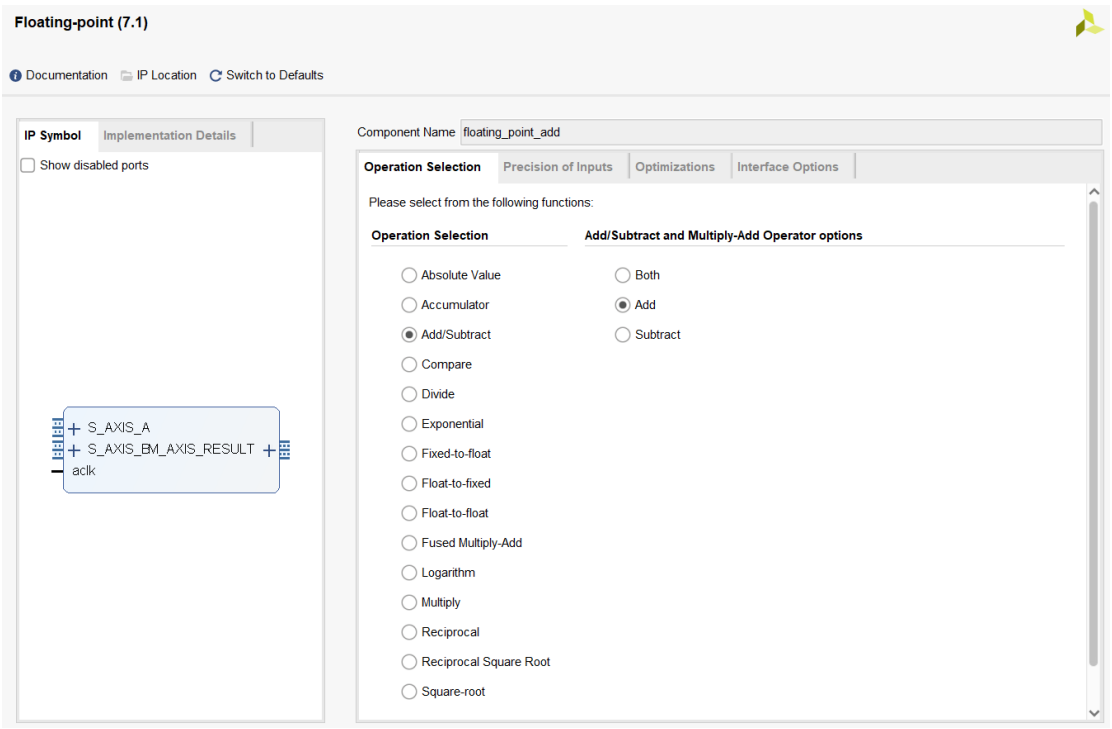


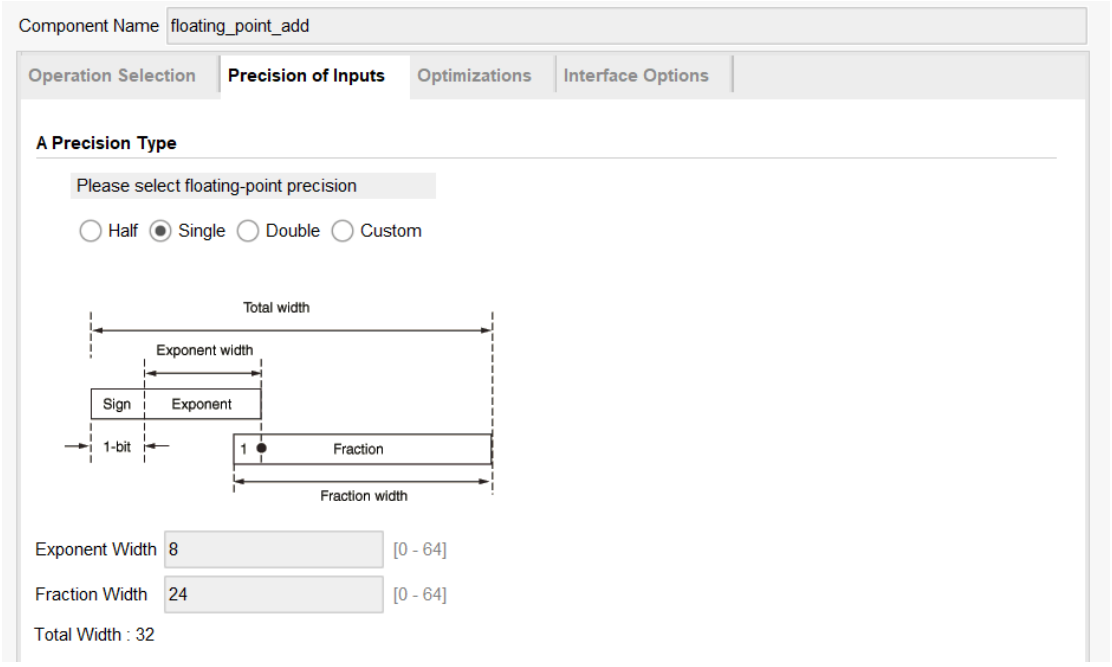

Component Name blk_mem_gen_0
Basic
Port A Options
Port B Options
Other Options
Summary
Memory Size
Port B Width 32
Port B Depth : 59904
The Width and Depth values are used for Read Operation in Port B
Operating Mode Write First
Enable Port Type Always Enabled
Port B Optional Output Registers
Primitives Output Register
Core Output Register
SoftECC Output Register
REGCEB Pin
Port B Output Reset Options
RSTB Pin (set/reset pin)
Output Reset Value (Hex) 0
Reset Memory Latch
Reset Priority CE (Latch or Register Enable)
READ Address Change B
Read Address Change B

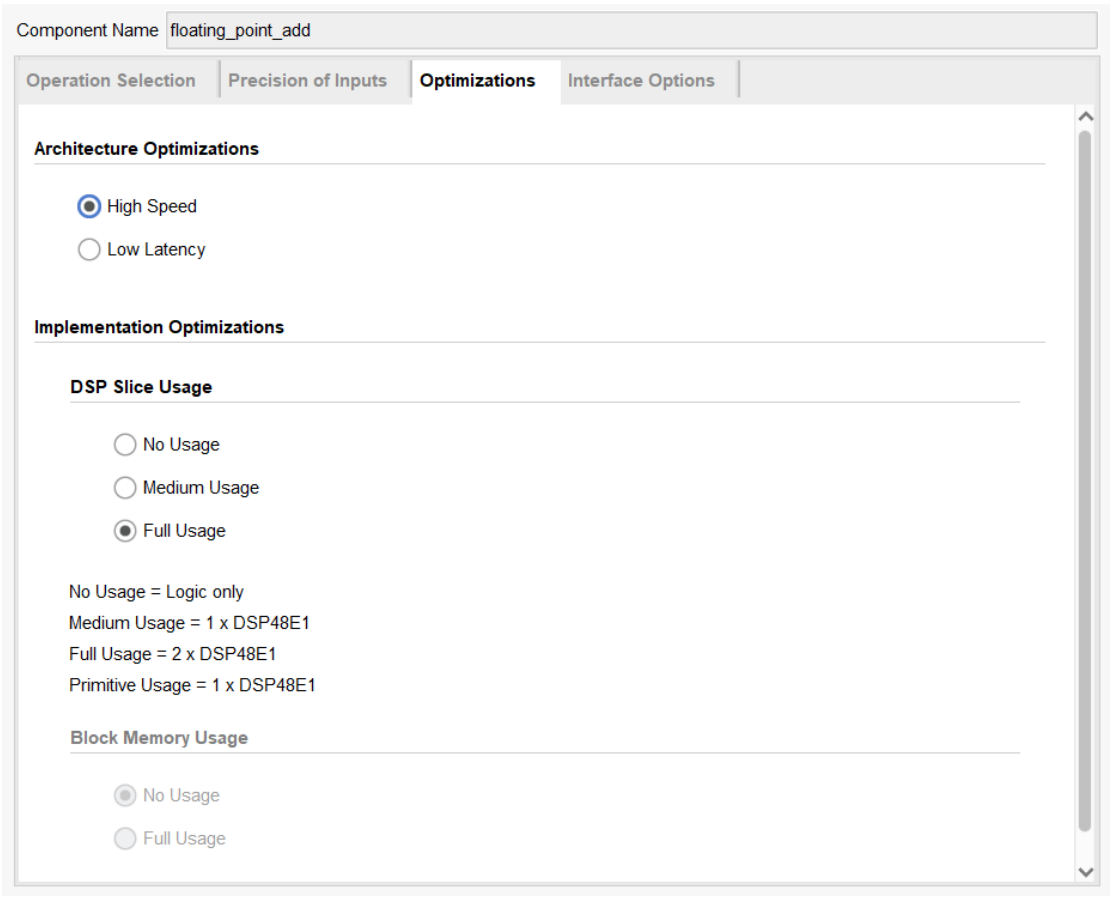

Component Name blk_mem_gen_0
Basic
Port A Options
Port B Options
Other Options
Summary
Pipeline Stages within Mux 0
Mux Size: 16x1
Memory Initialization
Load Init File
Coe File _ARM_CUP/5project/PicoSOC/hardware/facefinder.coe
Browse
Edit
Fill Remaining Memory Locations
Remaining Memory Locations (Hex) 0
Structural/UniSim Simulation Model Options
Defines the type of warnings and outputs are generated when a read-write or write-write collision occurs.
Collision Warnings All
Behavioral Simulation Model Options
Disable Collision Warnings
Disable Out of Range Warnings

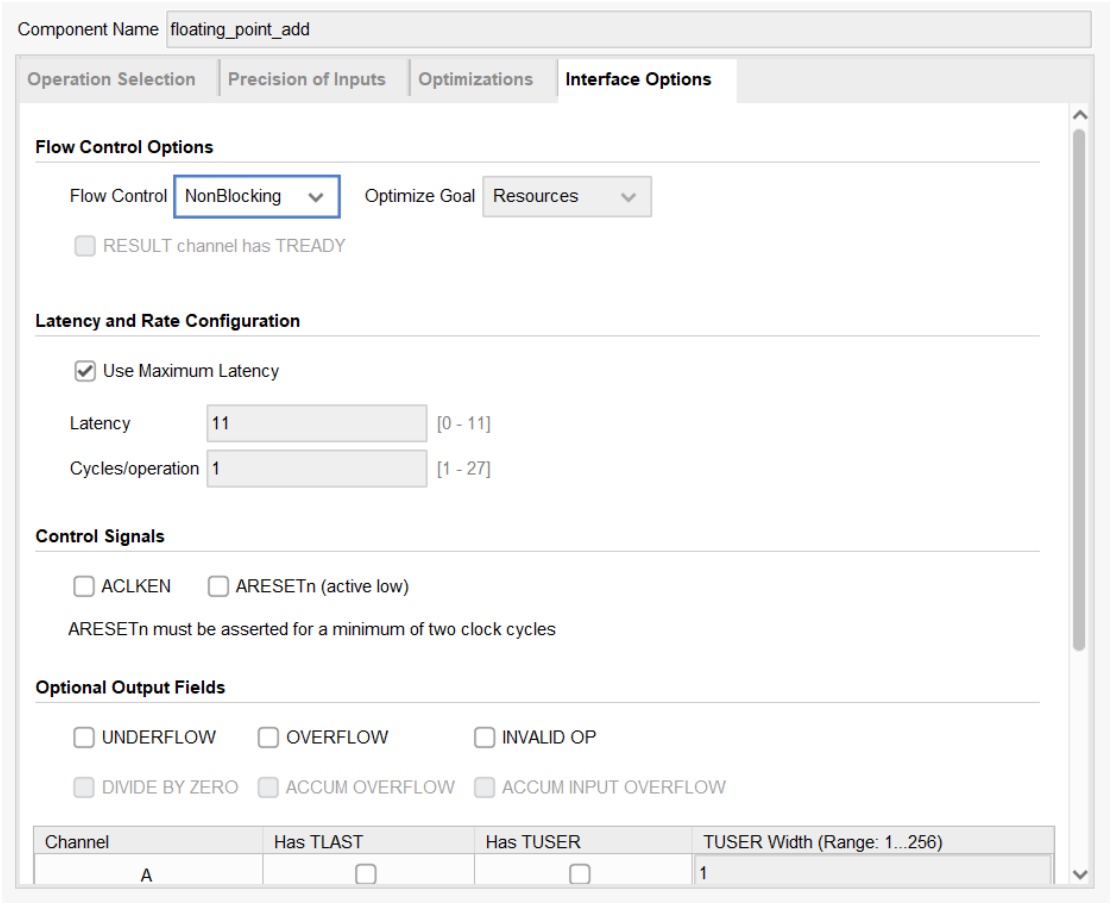

Component Name
blk_mem_gen_0
Basic
Port A Options
Port B Options
Other Options
Summary
Information
Memory Type: Dual Port ROM
Block RAM resource(s) (18K BRAMs): 10
Block RAM resource(s) (36K BRAMs): 49
Total Port A Read Latency : 1 Clock Cycle(s)
Total Port B Read Latency (From Rising Edge of Read Clock): 1 Clock Cycle(s)
Address Width A: 16
Address Width B : 16

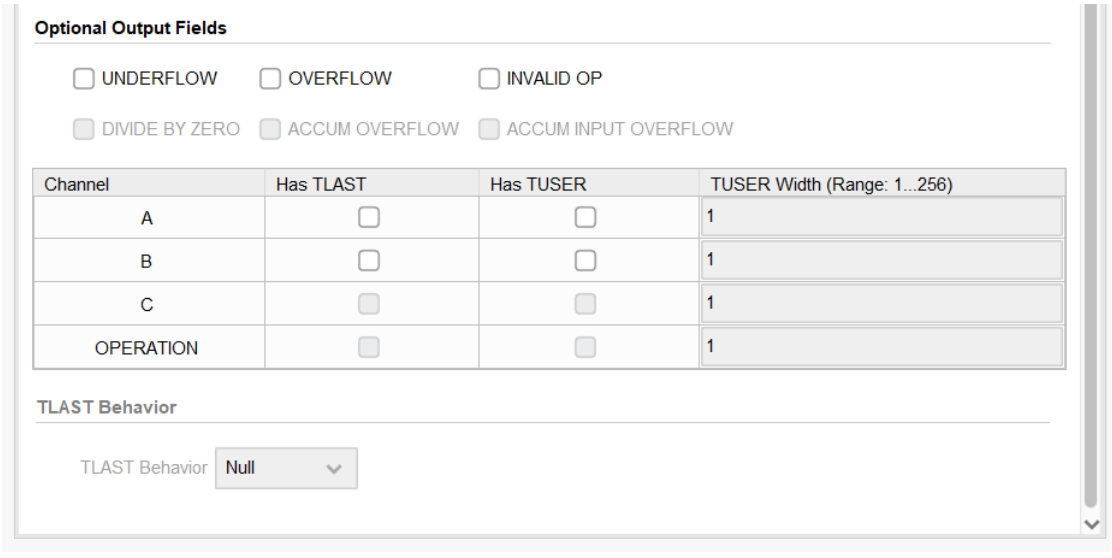
2.11 Floating-point-add



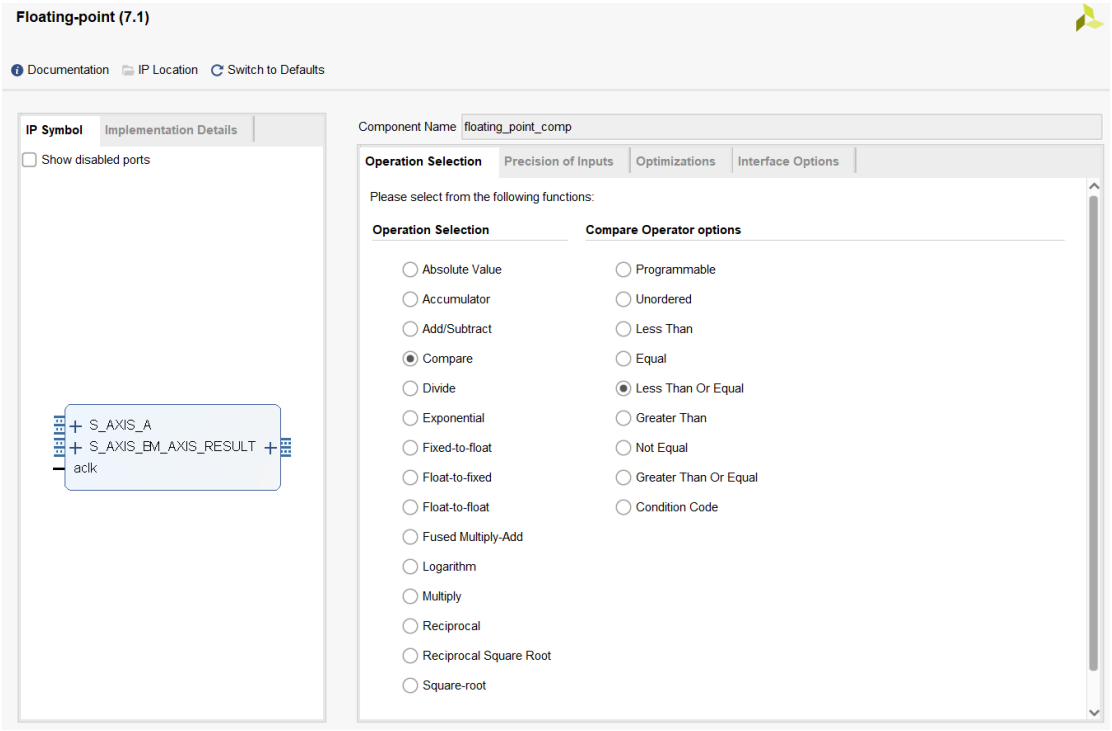


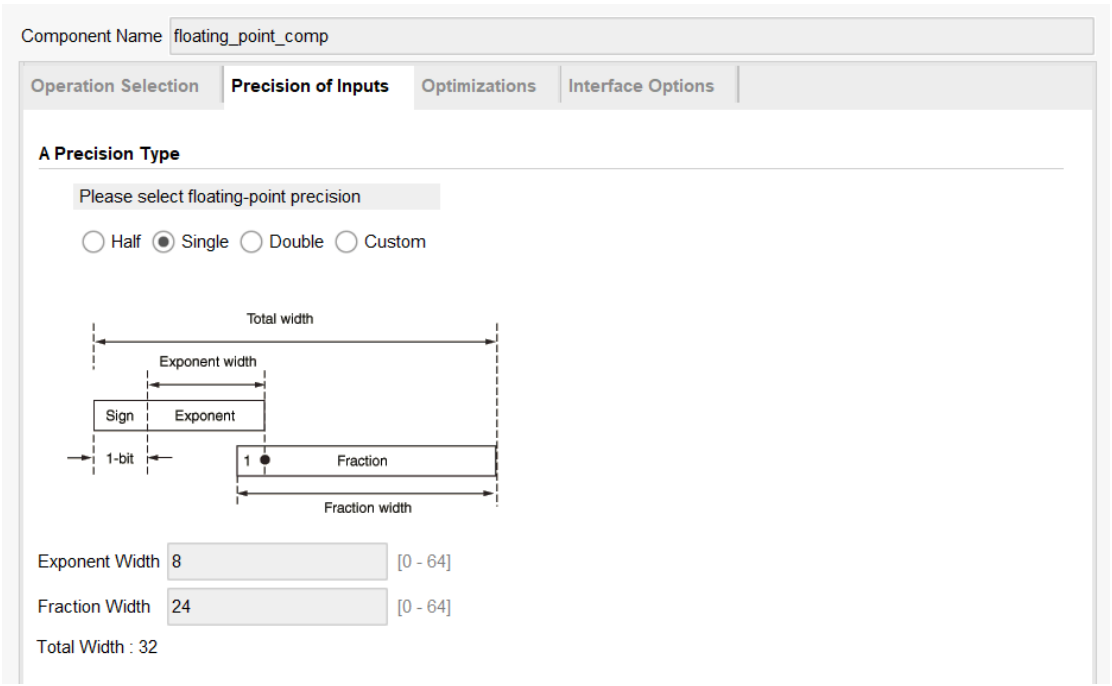

Component Name
floating_point_add
Operation Selection
Precision of Inputs
Optimizations
Interface Options
Architecture Optimizations
High Speed
Low Latency
Implementation Optimizations
DSP Slice Usage
No Usage
Medium Usage
Full Usage
No Usage = Logic only
Medium Usage = 1 x DSP48E1
Full Usage = 2 x DSP48E1
Primitive Usage = 1 x DSP48E1
Block Memory Usage
No Usage
Full Usage

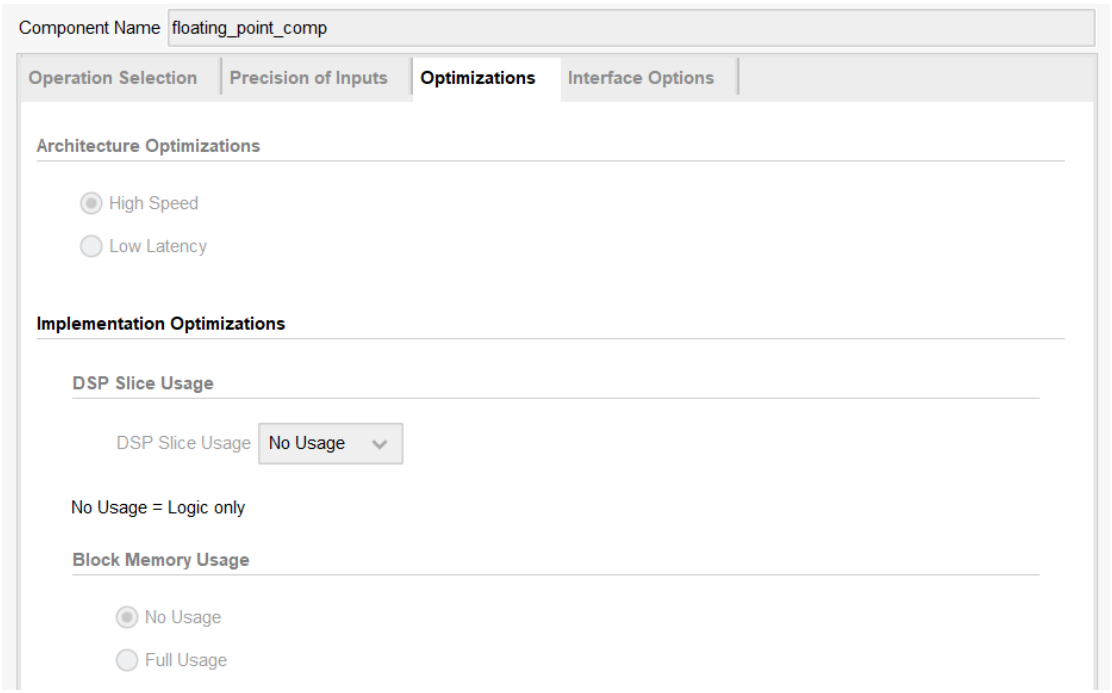

Component Name
floating_point_add
Operation Selection
Precision of Inputs
Optimizations
Interface Options
Flow Control Options
Flow Control
NonBlocking
Optimize Goal
Resources
RESULT channel has TREADY
Latency and Rate Configuration
Use Maximum Latency
Latency
11
[0 - 11]
Cycles/operation
1
[1 - 27]
Control Signals
ACLKEN
ARESETn (active low)
ARESETn must be asserted for a minimum of two clock cycles
Optional Output Fields
UNDERFLOW
OVERFLOW
INVALID OP
DIVIDE BY ZERO
ACCUM OVERFLOW
ACCUM INPUT OVERFLOW
Channel
Has TLAST
Has TUSER
TUSER Width (Range: 1...256)
A
1

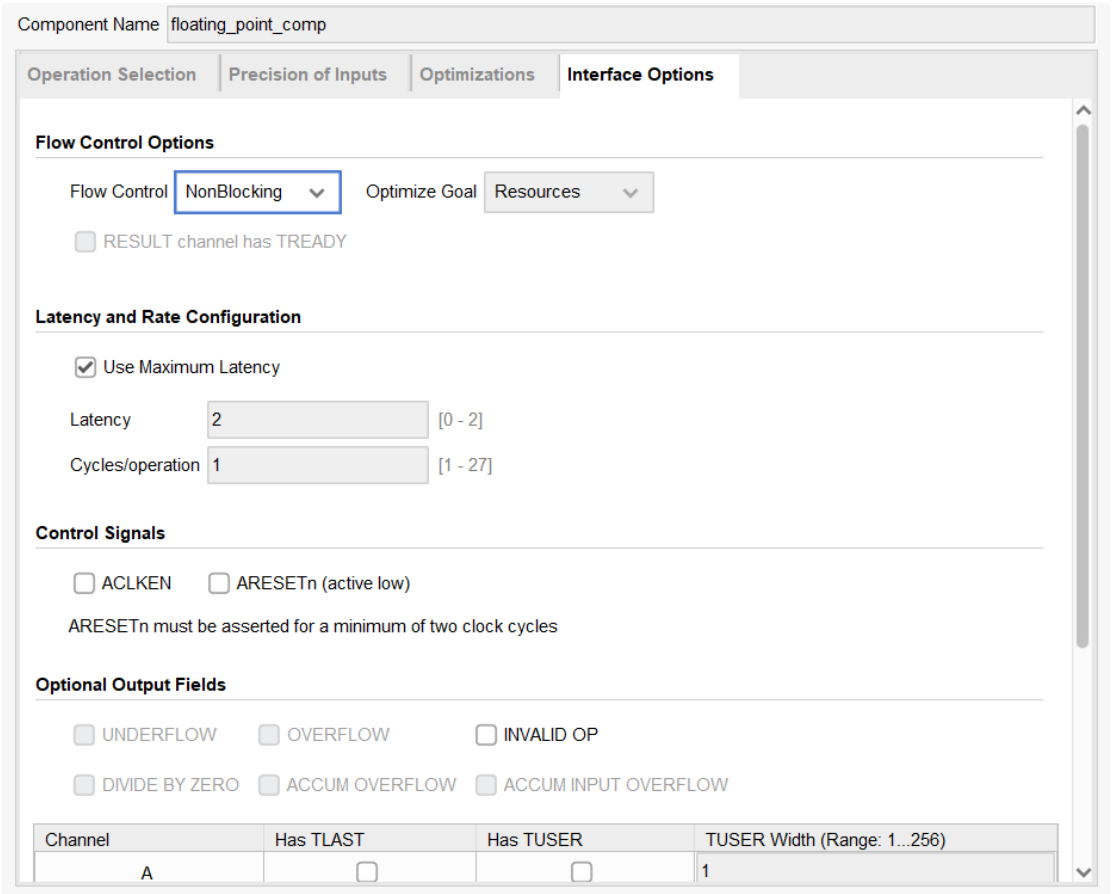

Optional Output Fields
UNDERFLOW
OVERFLOW
INVALID OP
DIVIDE BY ZERO
ACCUM OVERFLOW
ACCUM INPUT OVERFLOW
Channel
Has TLAST
Has TUSER
TUSER Width (Range: 1...256)
A
1
B
1
C
1
OPERATION
1
TLAST Behavior
TLAST Behavior
Null

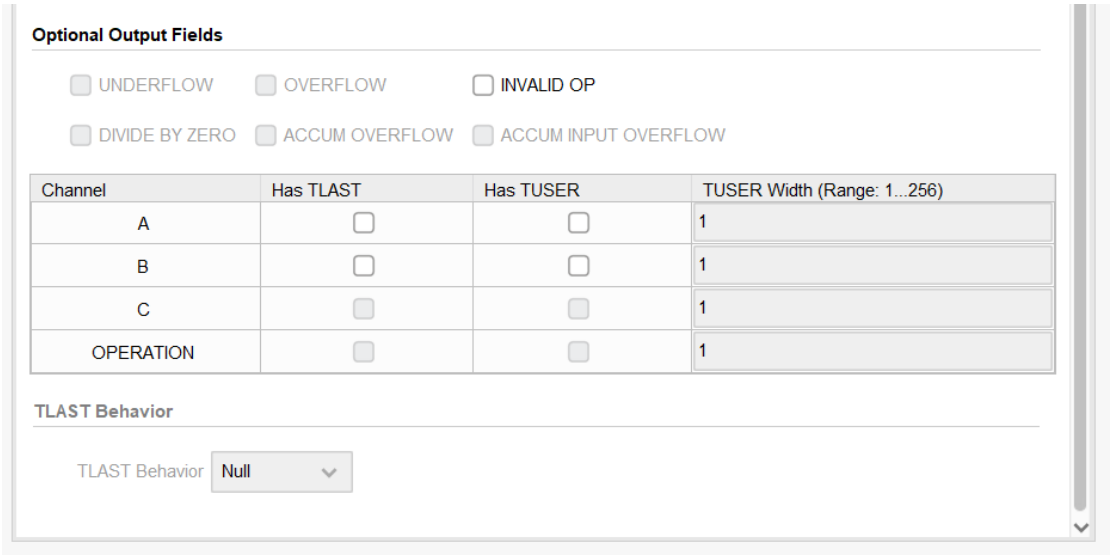
2.12 Floating-point-comp



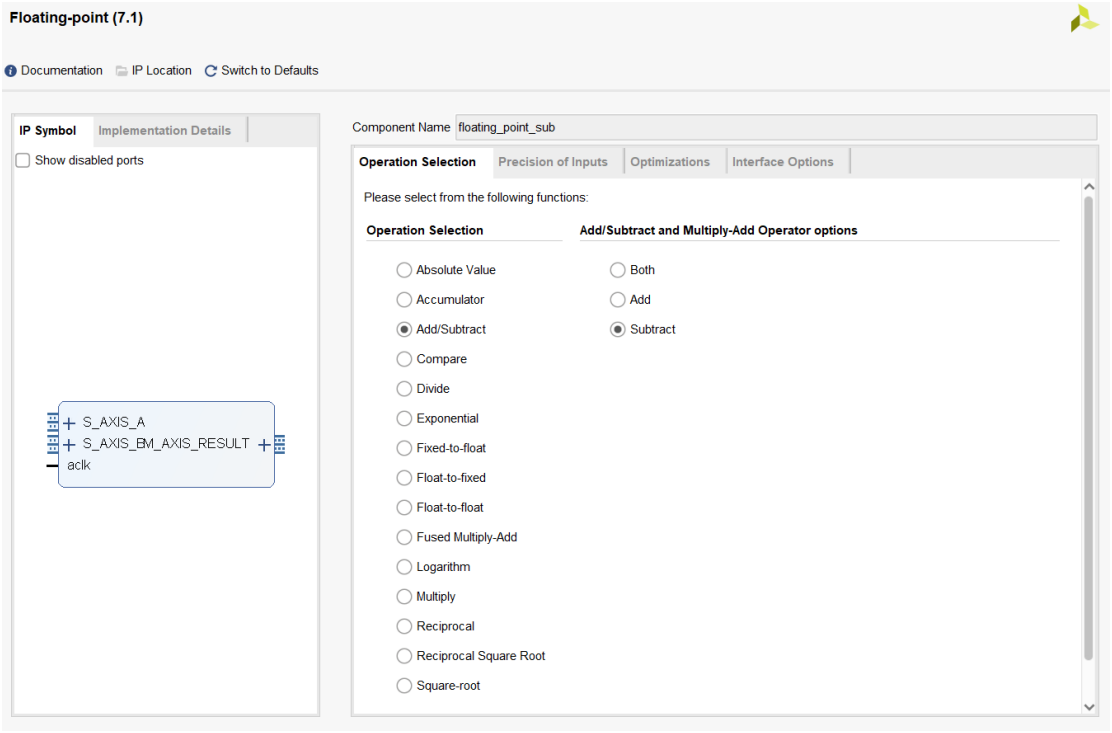


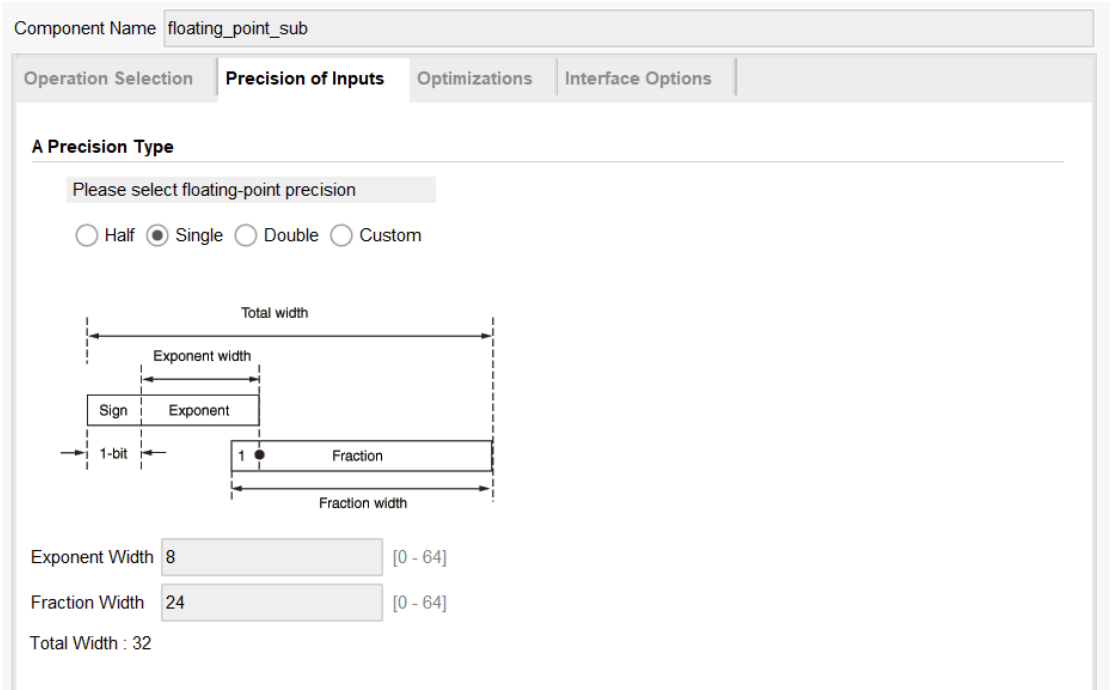

Component Name floating_point_comp
Operation Selection
Precision of Inputs
Optimizations
Interface Options
Architecture Optimizations
High Speed
Low Latency
Implementation Optimizations
DSP Slice Usage
DSP Slice Usage No Usage
No Usage = Logic only
Block Memory Usage
No Usage
Full Usage

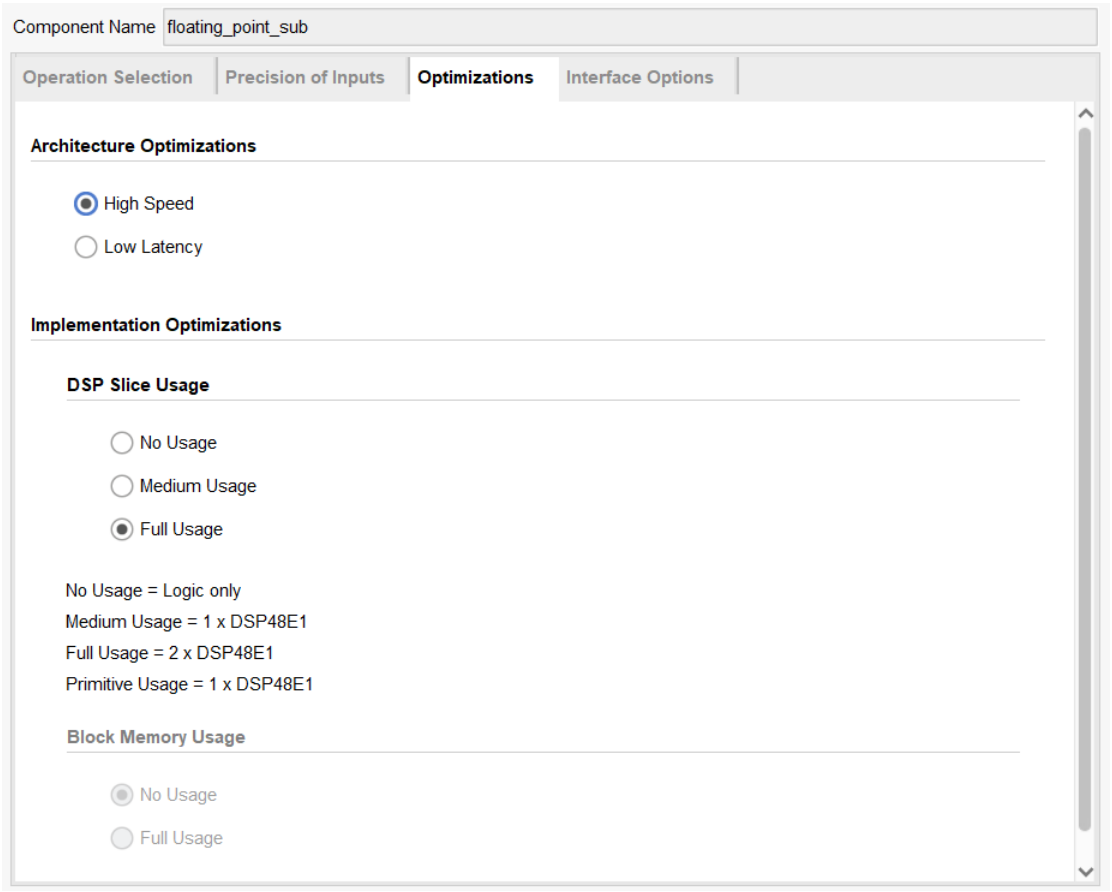

Component Name floating_point_comp
Operation Selection
Precision of Inputs
Optimizations
Interface Options
Flow Control Options
Flow Control NonBlocking
Optimize Goal Resources
RESULT channel has TREADY
Latency and Rate Configuration
Use Maximum Latency
Latency 2 [0 - 2]
Cycles/operation 1 [1 - 27]
Control Signals
ACLKEN
ARESETn (active low)
ARESETn must be asserted for a minimum of two clock cycles
Optional Output Fields
UNDERFLOW
OVERFLOW
INVALID OP
DIVIDE BY ZERO
ACCUM OVERFLOW
ACCUM INPUT OVERFLOW
Channel
Has TLAST
Has TUSER
TUSER Width (Range: 1...256)
A
1

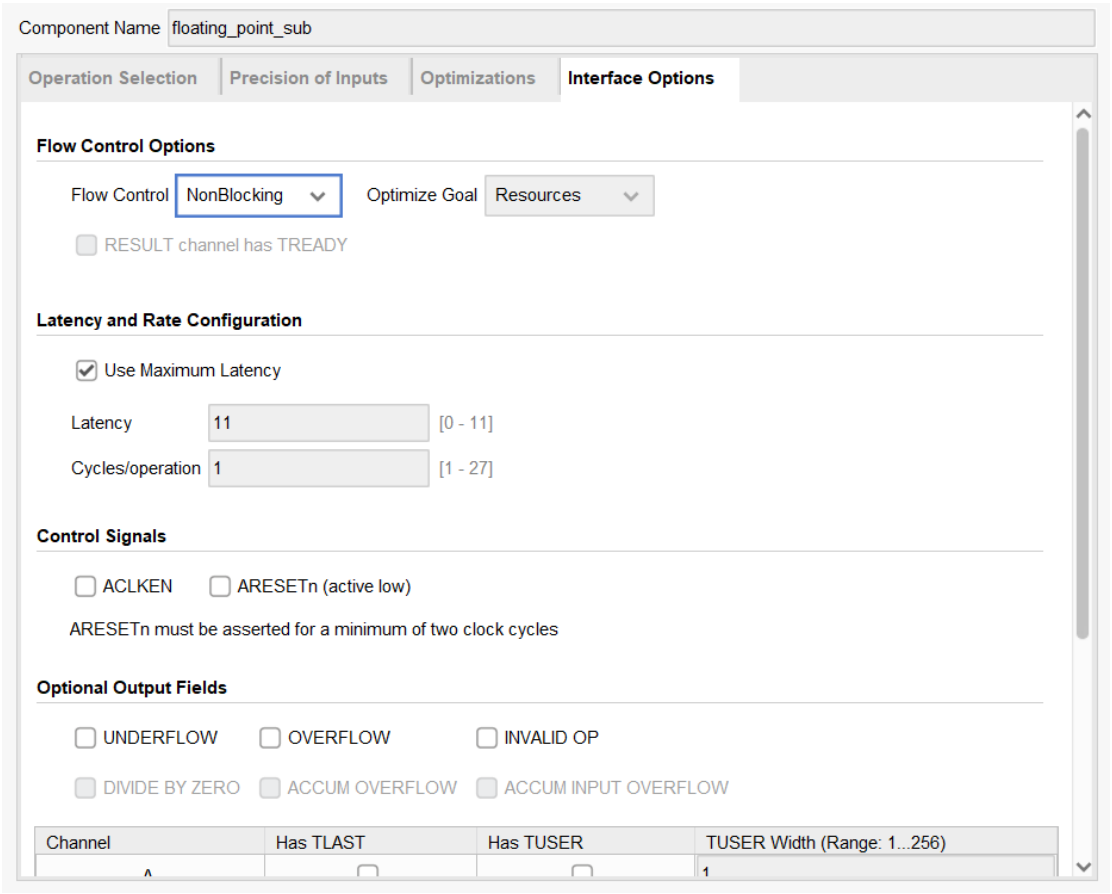

Optional Output Fields
UNDERFLOW
OVERFLOW
INVALID OP
DIVIDE BY ZERO
ACCUM OVERFLOW
ACCUM INPUT OVERFLOW
Channel
Has TLAST
Has TUSER
TUSER Width (Range: 1...256)
A
1
B
1
C
1
OPERATION
1
TLAST Behavior
TLAST Behavior
Null

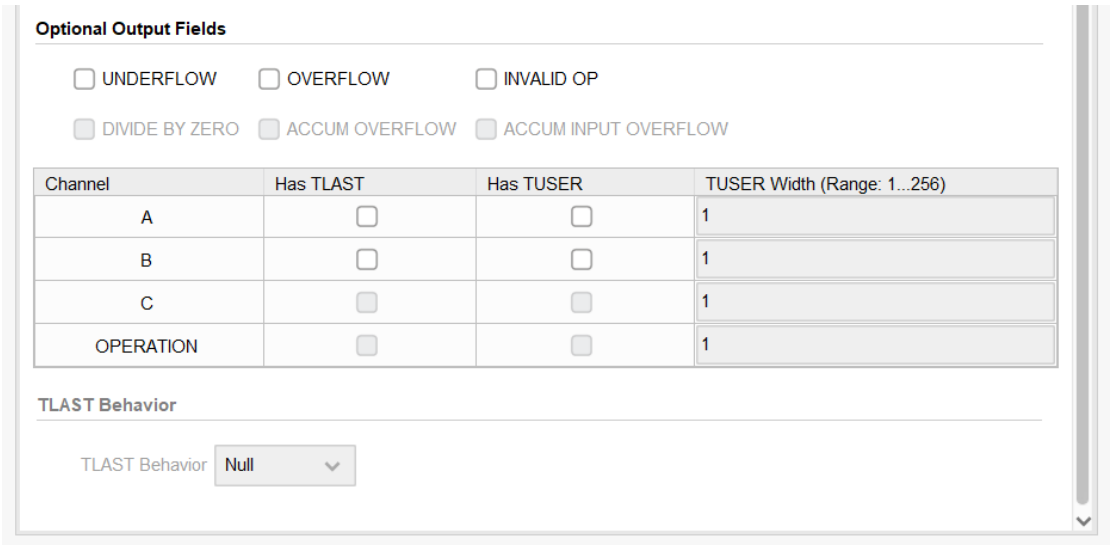
2.13 Floating-point-sub






Component Name
floating_point_sub
Operation Selection
Precision of Inputs
Optimizations
Interface Options
Architecture Optimizations
High Speed
Low Latency
Implementation Optimizations
DSP Slice Usage
No Usage
Medium Usage
Full Usage
No Usage = Logic only
Medium Usage = 1 x DSP48E1
Full Usage = 2 x DSP48E1
Primitive Usage = 1 x DSP48E1
Block Memory Usage
No Usage
Full Usage


Component Name floating_point_sub
Operation Selection
Precision of Inputs
Optimizations
Interface Options
Flow Control Options
Flow Control NonBlocking
Optimize Goal Resources
RESULT channel has TREADY
Latency and Rate Configuration
Use Maximum Latency
Latency 11 [0 - 11]
Cycles/operation 1 [1 - 27]
Control Signals
ACLKEN
ARESETn (active low)
ARESETn must be asserted for a minimum of two clock cycles
Optional Output Fields
UNDERFLOW
OVERFLOW
INVALID OP
DIVIDE BY ZERO
ACCUM OVERFLOW
ACCUM INPUT OVERFLOW
Channel
Has TLAST
Has TUSER
TUSER Width (Range: 1...256)


Optional Output Fields
UNDERFLOW
OVERFLOW
INVALID OP
DIVIDE BY ZERO
ACCUM OVERFLOW
ACCUM INPUT OVERFLOW
Channel
Has TLAST
Has TUSER
TUSER Width (Range: 1...256)
A
B
C
OPERATION
TLAST Behavior
TLAST Behavior Null

第三章　串口