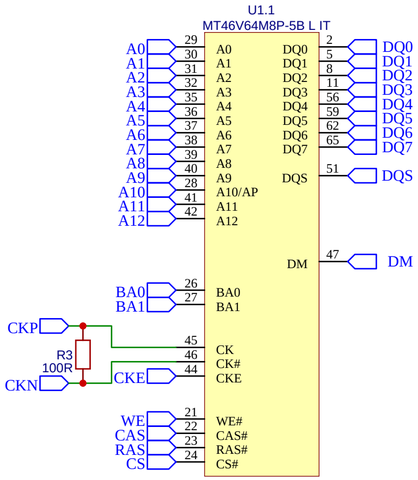

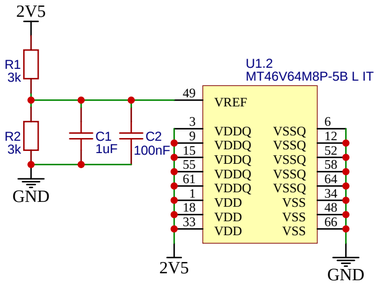

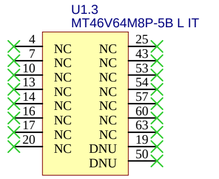

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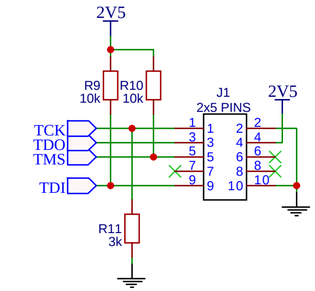
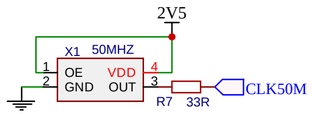


FPGA JTAG接口



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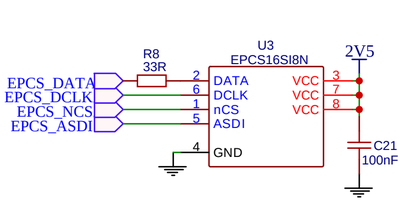
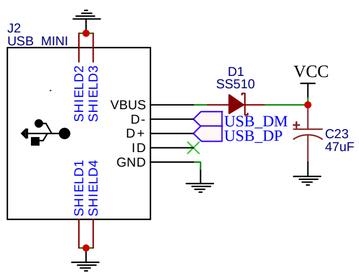
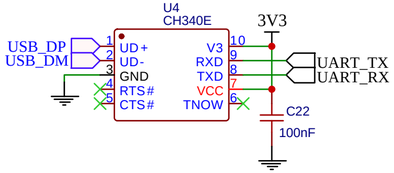
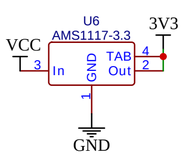


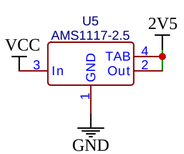
配置存储芯片

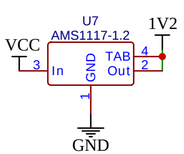


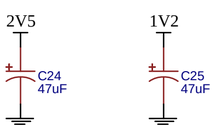


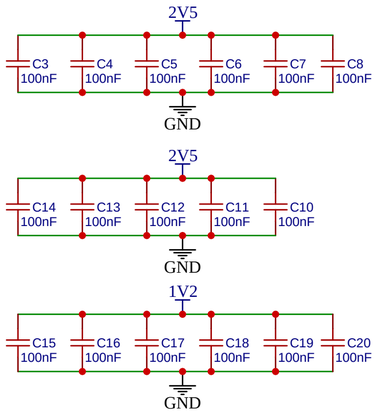
USB-UART

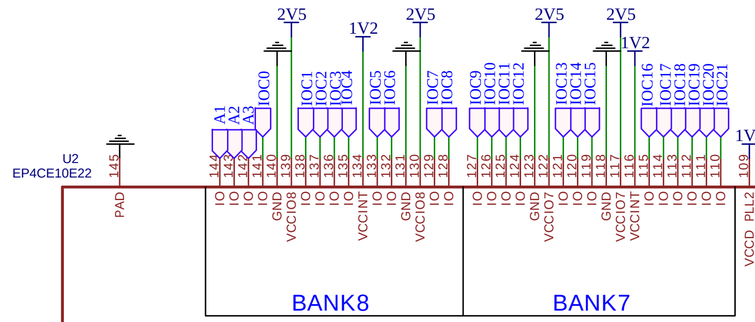


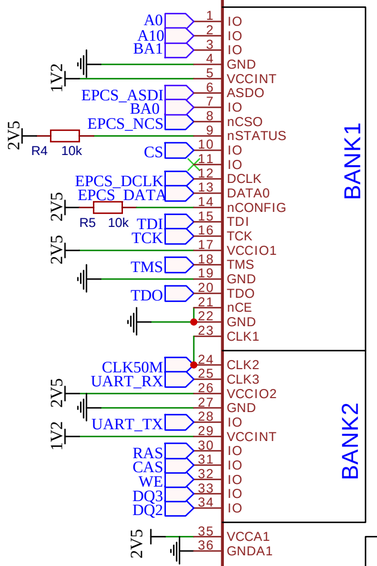


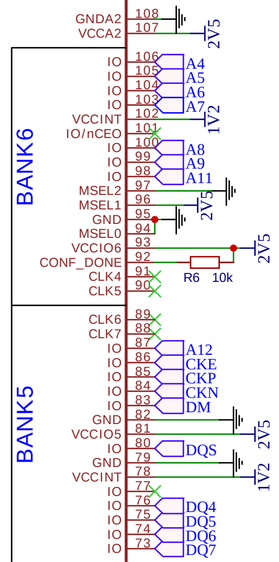






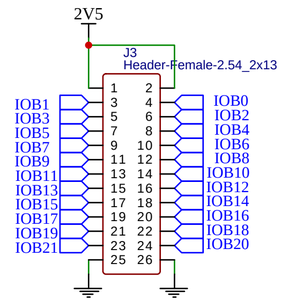


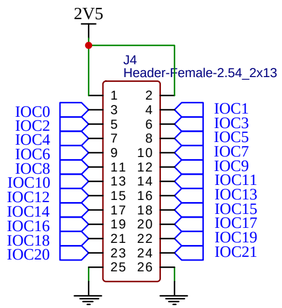




ALTERA
Cyclone IV
EP4CE10E22

FPGA





TITLE: FPGA+DDR	REV: 1.0
Company: Your Company	Sheet: 1/1
Date: 2020-02-09 Drawn By: wangxuan	

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