PacoBlaze

Version 2006-03-14

What is PacoBlaze and KCAsm?

PacoBlaze is a from-scratch synthesizable & behavioral Verilog clone of Ken Chapman's popular PicoBlaze embedded microcontroller. KCAsm is a lightweight PicoBlaze assembler written in Java.

Why does PacoBlaze exist?

While Ken's version aims toward the most efficient implementation in the Xilinx FPGA architecture, PacoBlaze tries to be as device-independent as possible maintaining source code compatibility and code cycle accuracy with the original PicoBlaze. Moreover, as there are actually 3 versions of the PicoBlaze microcontroller, PacoBlaze's final achievement is to provide all PicoBlaze versions in one configurable Verilog file set.

The nice thing™ of having a behavioral Verilog model of PicoBlaze is that it is easier to modify, trim or expand the core in order to adapt it for special purpose applications (e.g. PacoBlaze mods with a multiply or bit count instructions). It also makes pure behavioral Verilog simulations possible; something really neat that has allowed many of its users to reach Nirvana.

Who wrote it and why?

Pablo Bleyer Kocik, yours truly. I started working in PacoBlaze because I was in need of a small embedded controller for my FPGA-based projects and, even I was a big fan of the original PicoBlaze, it's lack of configurability was restraining my creativity... No, really.

PacoBlaze has been written for Verilog-2001 compliance and is tested with Stephen Williams' Icarus Verilog compiler and Pragmatic C's GPL Cver compiler. Xilinx ISE WebPACK is used for testing core synthesis, including module inference. KCAsm is compiled and tested using Sun's J2SE JDK and utilizes the JavaCC Java compiler-compiler.

What is PacoBlaze's license?

PacoBlaze and KCAsm are released under the BSD License for maximum flexibility and usefulness. This means you can use the project however you wish, without compromising your whole project and liberating me from any responsibilities (so both of us can have peaceful dreams). A copy of the license is included at the end of this document. Although you are not legally bound, it is considered morally and socially acceptable if you send me back bug reports.

Files

File name	Description
Makefile	Makefile with rules to build the simulations for the distribution.
pacoblaze_inc.v	Main include file for definitions and macros.
pacoblaze.v	Main PacoBlaze module file, parametrized with macros.
pacoblaze_idu.v	Instruction Decode Unit implementation.
pacoblaze_register.v	Register file implementation.
pacoblaze_stack.v	Address stack implementation.
pacoblaze_scratch.v	Scratchpad implementation.
pacoblaze_util.v	Code utilities.
pacoblaze{1,2,3}.v	PacoBlaze 1, 2 or 3 module definition. You should use this for each PacoBlaze instantiation.
pacoblaze{1,2,3}_xst.v	Module instantiation with relative paths that I use for XST synthesis (since XST doesn't currently allow specifying Verilog include directories. Arrrgh!).
blockram.v	Behavioral BlockRAM description for synthesis.

Other files

File name	Description
pacoblaze_dregister.v	Dual register file implementation (even/odd and dual register accesses).
X_tb.v	Testbenches.

Macros

Macro name	Description
PACOBLAZE{1,2,3}	Define this before including pacoblaze_inc.v to specify which PacoBlaze configuration to use.
HAS_RESET_LATCH	When defined, the reset signal drives an internal reset to avoid reset glitches.
USE_ONEHOT_ENCODING	Use one-hot encoding for opcode decoding.
HAS_INTERRUPT_ACK	Export interrupt acknowledge signal in the top module.
HAS_SCRATCH_MEMORY	Enable resources for scratchpad memory implementation.
HAS_COMPARE_OPERATION	Enable the “compare” operation.
HAS_TEST_OPERATION	Enable the “test” operation.
HAS_DEBUG	When defined will export debugging signals.

Extensions

Macro name	Description
HAS_MUL_OPERATION	Enable the 8x8 multiply operation.

Using KCAsm

The command line to assembly the KCPSM3-psm file *my_assembler_file.psm* and create the *my_module_name.v* 18-bit BlockRAM Verilog configuration file together with the *my_listing_file.rmh* Verilog-readmemh listing file, is:

```
java -Dkcpsm=3 -Dbram=18 -Dmodule=my_module_name -jar KCAsm.jar
my_assembler_file.psm my_listing_file.rmh
```

PicoBlaze resources

- PicoBlaze @ Xilinx
- PicoBlaze Product Brief
- PicoBlaze User Resources
- TechXclusives: Creating Embedded Microcontrollers (Programmable State Machines) by Ken Chapman [PDF]
- Xilinx UG129 PicoBlaze 8-bit Embedded Microcontroller for Spartan-3, Virtex-II, and Virtex-II Pro FPGAs
- FPGA IFF Copy Protection Using Dallas Semiconductor/Maxim DS2432 Secure EEPROMs
- PicoBlaze 8-Bit Microcontroller for Virtex-II Series Devices
- Reducing the Size of SD-SDI EDH Processing Using the PicoBlaze Processor
- Multi-Rate SDI Integration Examples for the Serial Digital Video Demonstration Board
- Embedded Processing and Control Solutions for Spartan-3 FPGAs
- On the Fly Reconfiguration with CoolRunner-II CPLDs
- PicoBlaze 8-Bit Microcontroller for CPLD Devices [ZIP]
- CryptoBlaze: 8-Bit Security Microcontroller [ZIP]
- PicoBlaze 8-Bit Microcontroller for Virtex-E and Spartan-II/IIE Devices
- DVI, VGA, and Component Video Demonstration
- pBlaze IDE - an Integrated Development Environment dedicated to the KCPSM soft core
- kpicosim - a development environment for the Xilinx PicoBlaze-3 soft-core processor for the KDE Desktop
- Enterpoint's Picoblaze Enhancements

Contributors

Here are some recent kind users which have helped identifying bugs and petted PacoBlaze with affection.

- Allan Herriman
- Ed Blanchard

Please contact me if I have forgotten you and you wish to be added to the list.

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