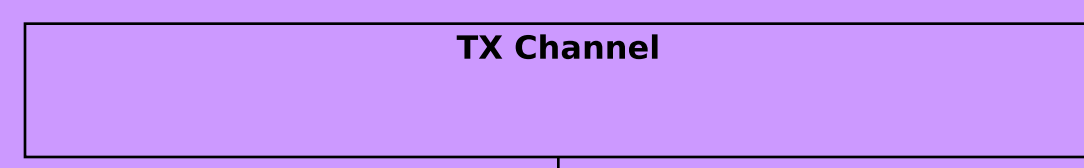
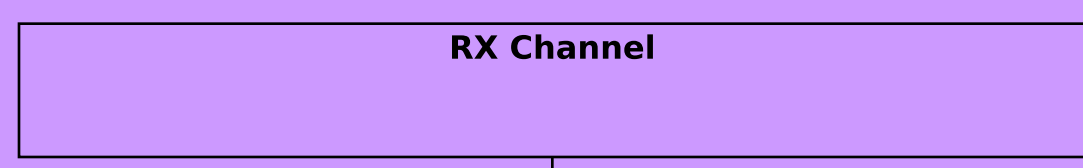
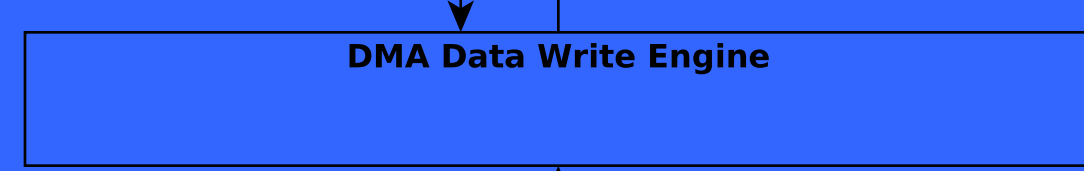
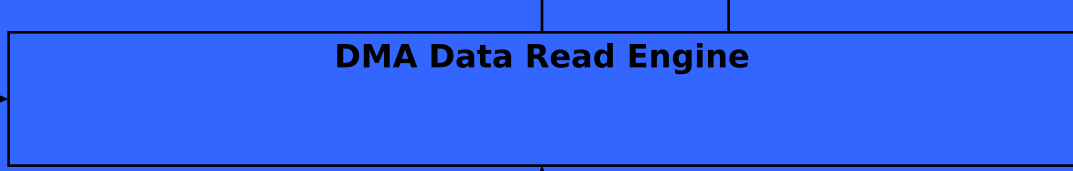
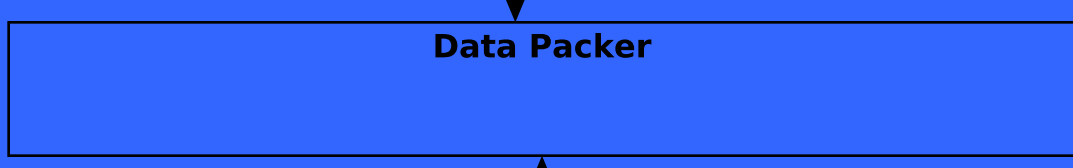


# User Application

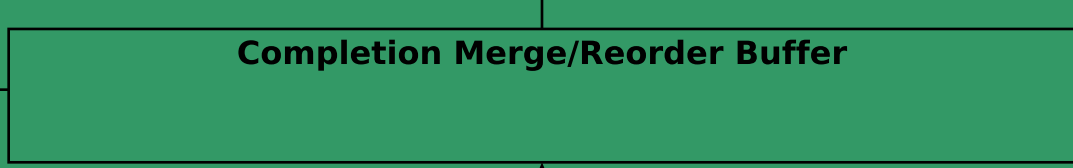
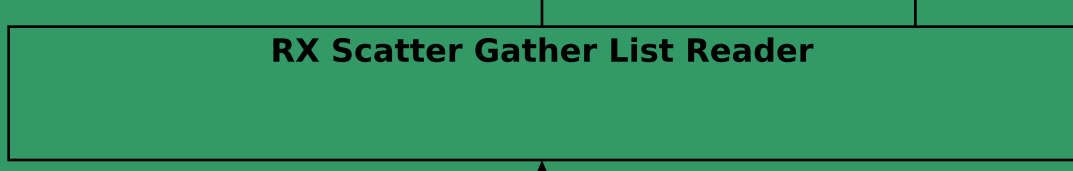
## Channel Interface (RIFFA)



## Data Abstraction / DMA Layer (RIFFA)



## SG DMA Layer



RX Request (RxR) Interface

Rx Completion (RxC) Interface

Interrupt Interface

Config Interface

Tx Completion (TxC) Interface

Tx Request (TxR) Mux

## Engine Layer

RX Request (RxR) Interface

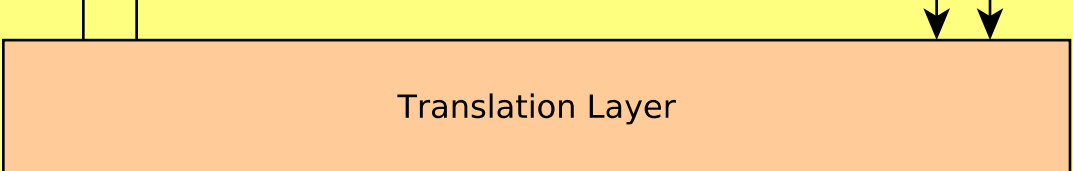
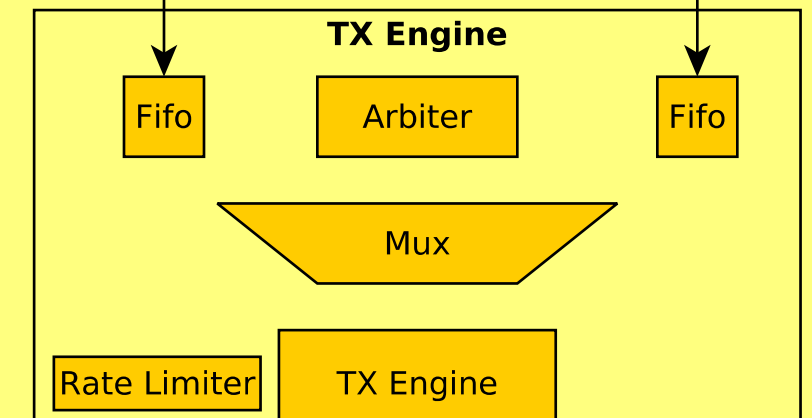
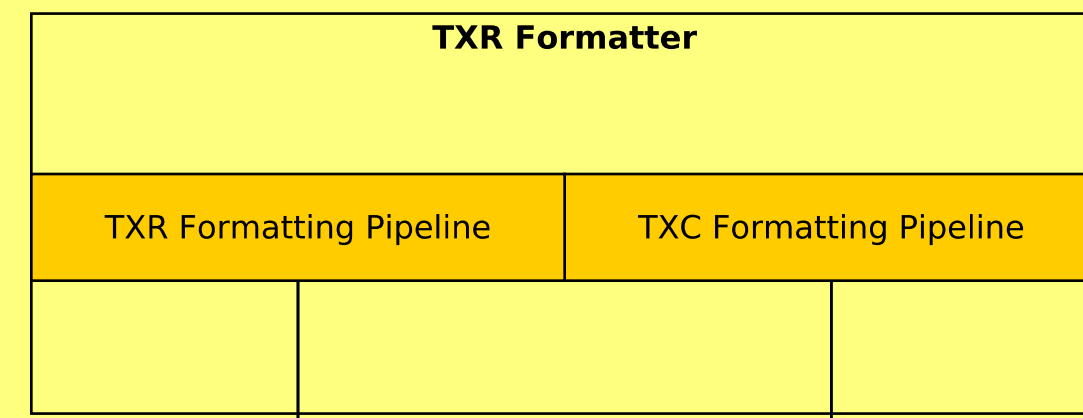
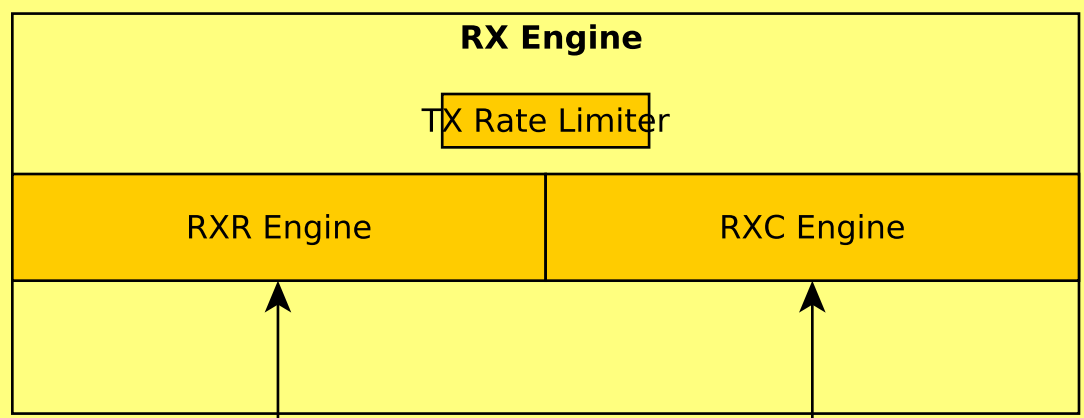
Rx Completion (RxC) Interface

Interrupt Engine

Config Interface

Tx Completion Interface

Tx Request Interface



## Xilinx Ultrascale Core

