User Application

Channel Interface (RIFFA)

RX Channel

TX Channel

Data Abstraction / DMA Layer (RIFFA)

Data Packer

Write Buffer

DMA Data Read Engine

DMA Data Write Engine

SG DMA Layer

RX Scatter Gather List Reader

TX Scatter Gather List Reader

Completion Merge/Reorder Buffer

BAR Memory Space

RX Request (RxR) Interface

Rx Completion (RxC)

Interrupt Interface

Config Interface

Tx Completion (TxC)

Tx Request (TxR) Mux

RXR_DATA[C_PCI_DWIDTH-1:0]
RXR_DATA_VALID
RXR_DATA_READY
RXR_TC[2:0]
RXR_ATTR[2:0]
RXR_TAG[7:0]
RXR_REQUEST_TYPE[3:0]
RXR_ADDR[63:0]
RXR_BAR_DECODED[8:0]
RXR_REQUESTER_ID[15:0]
RXR_LENGTH[10:0]
RXR_DATA_START_FLAG
RXR_DATA_START_OFFSET[3:0]
RXR_DATA_FDWBE[3:0]
RXR_DATA_END_FLAG
RXR_DATA_END_OFFSET[3:0]
RXR_DATA_LDWBE[3:0]

RXC_DATA[C_PCI_DWIDTH-1:0]
RXC_DATA_VALID
RXC_DATA_READY
RXC_META_TAG[7:0]
RXC_META_ADDR[7:0]
RXC_META_LENGTH[9:0]
RXC_META_BYTES_REMAINING[12:0]
RXC_META_COMPLETER_ID[15:0]
RXC_DATA_START_FLAG
RXC_DATA_START_OFFSET[3:0]
RXC_DATA_FDWBE[3:0]
RXC_DATA_END_FLAG
RXC_DATA_END_OFFSET[3:0]
RXC_DATA_LDWBE[3:0]

INTR_MSI_REQUEST
INTR_MSI_NUMBER[4:0]
INTR_MSI_ACK

CONFIG_COMPLETER_ID
CONFIG_BUS_MASTER_ENABLE
CONFIG_LINK_WIDTH
CONFIG_LINK_RATE
CONFIG_MAX_READ_REQUEST
CONFIG_MAX_PAYLOAD
CONFIG_MSIENABLE

TXC_DATA[C_PCI_DWIDTH-1:0]
TXC_DATA_VALID
TXC_DATA_READY
TXC_DATA_START_FLAG
TXC_DATA_START_OFFSET[3:0]
TXC_DATA_FDWBE[3:0]
TXC_DATA_END_FLAG
TXC_DATA_END_OFFSET[3:0]
TXC_DATA_LDWBE[3:0]
TXC_META_ADDR[7:0]
TXC_META_LENGTH[8:0]
TXC_META_BYTE_COUNT[12:0]
TXC_META_TAG[8:0]
TXC_META_REQUESTER_ID[15:0]
TXC_META_TC[2:0]
TXC_META_ATTR[2:0]
TXC_META_EP

TXR_DATA[C_PCI_DWIDTH-1:0]
TXR_DATA_VALID
TXR_DATA_READY
TXR_DATA_START_FLAG
TXR_DATA_START_OFFSET[3:0]
TXR_DATA_FDWBE[3:0]
TXR_DATA_END_FLAG
TXR_DATA_LDWBE[3:0]
TXR_DATA_END_OFFSET[3:0]
TXR_META_ADDR[63:0]
TXR_META_LENGTH[9:0]
TXR_META_TAG[2:0] (Virtualized)
TXR_META_TC[2:0]
TXR_META_ATTR[2:0]
TXR_META_TYPE[3:0]
TXR_META_EP

Engine Layer

RX Request (RxR) Interface

Rx Completion (RxC) Interface

Interrupt Engine

Config Interface

Tx Completion Interface

Tx Request Interface

RX Engine

TX Rate Limiter

RXR Engine

RXC Engine

TXR Formatter

TXR Formatting Pipeline

TXC Formatting Pipeline

TX Engine

Fifo

Arbiter

Fifo

Mux

Rate Limiter

TX Engine

Translation Layer

CQ
RC

RQ
CC

Xilinx Ultrascale Core

RX_TLP[C_PCI_DWIDTH-1:0]
RX_TLP_READY
RX_TLP_VALID
RX_TLP_START_FLAG
RX_TLP_START_OFFSET[3:0]
RX_TLP_END_FLAG
RX_TLP_END_OFFSET[3:0]
RX_TLP_BAR_DECODE[7:0]

CONFIG_MSI_ENABLE
CONFIG_MAX_READ_REQUEST
CONFIG_MAX_PAYLOAD
CONFIG_LINK_RATE
CONFIG_LINK_WIDTH
CONFIG_BUS_MASTER_ENABLE
CONFIG_COMPLETER_ID

INTR_LEGACY_READY
INTR_MSI_READY
INTR_MSI_REQUEST
INTR_MSI_NUM[4:0]
INTR_LEGACY_REQUEST

TX_TLP[C_PCI_DWIDTH-1:0]
TX_TLP_VALID
TX_TLP_READY
TX_TLP_START_FLAG
TX_TLP_START_OFFSET[3:0]
TX_TLP_END_OFFSET[3:0]
TX_TLP_END_FLAG

Translation Layer

M_AXIS_RX_TDATA[C_PCI_DWIDTH-1:0]
M_AXIS_RX_TREADY
M_AXIS_RX_TVALID
IS_SOF[3:0] (128 only)
M_AXIS_RX_TLAST
IS_EOF[3:0] (128 Only)
RERR_FWD
M_AXIS_RX_TKEEP[(C_PCI_DWIDTH/8)-1:0]

INTR_LEGACY_CLR
CFG_INTERRUPT_ASSERT
CFG_INTERRUPT_RDY
CFG_INTERRUPT
CFG_MSI_NUM[4:0]

COMPLETER_ID
CFG_BUS_MSTR_ENABLE
CFG_LINK_WIDTH
CFG_LINK_RATE
MAX_PAYLOAD_SIZE
MAX_READ_REQUEST_SIZE
CFG_INTERRUPT_MSIENABLE

S_AXIS_TX_TDATA[C_PCI_DWIDTH-1:0]
S_AXIS_TX_TREADY
S_AXIS_TX_TVALID
S_AXIS_TX_TLAST
S_AXIS_SRC_DSC
S_AXIS_TX_TKEEP[(C_PCI_DWIDTH/8)-1:0]

PCIe Core (Xilinx Gen1,2)

RX Interface

Interrupt Interface

Config Interface

TX Interface

RX_ST_DATA[C_PCI_DWIDTH-1:0]
RX_ST_READY
RX_ST_VALID
RX_ST_SOP[1:0]
RX_ST_EOP[1:0]
RX_ST_EMPTY[1:0]

APP_INT_ACK
APP_MSI_ACK
APP_INT_STS
APP_MSI_REQ

TL_CFG_CTL[21:0]
TL_CFG_ADD[4:0]
TL_CFG_STS[52:0]
CURRENTSPEED[1:0]

TX_ST_DATA[C_PCI_DWIDTH-1:0]
TX_ST_READY
TX_ST_VALID
TX_ST_EMPTY[1:0]
TX_ST_EOP
TX_ST_SOP

PCIe Core (Altera Gen 1,2,3)

RX Interface

Interrupt Interface

Config Interface

TX Interface